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InAs Device Process Development and Characterization

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14. ABSTRACT

This report summarizes the results of the initial effort in InAs bipolar device development. InAs is one of the III-V semiconductor materials exhibiting a relatively small energy bandgap and extremely high electron mobility, properties both desirable for high-frequency, low-power dissipation device applications. The major accomplishment of this work is the development of a robust device fabrication process that can be directly transferred to an industrial environment. Ti/Pt/Au was used as a universal *n*- and *p*- type contact with record low contact resistances. For the base access etch, which is one of the critical issues for bipolar device processing, a unique doping dependence etch was discovered for InAs that allows the base access etch to stop at the appropriate layer. The low-bandgap InAs and heavy doping resulted in premature breakdown through current tunneling and uncontrollable reverse leakage current. This effect was addressed successfully through interactive MBE growth, device characterization, and material analysis techniques. *Pn* junctions, the building blocks for bipolar transistors were produced with reverse leakage current as low as 10 μA at ⍈1 V and breakdown voltages as high as 6.5 V. The InAs *pn* junctions produced had promising rectifying diode characteristics for low-voltage operation and high-speed current amplifier applications.

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InAs DEVICE PROCESS DEVELOPMENT AND CHARACTERIZATION

1. SUMMARY

This report summarizes the results of the initial effort in InAs device development at the Naval Research Laboratory (NRL) performed between 1999 and 2000. The major accomplishments are the development of a robust device fabrication process that can be directly transferred to an industrial environment. Ti/Pt/Au was used as a universal *n*- and *p*-type contact with record low contact resistances. For the base access etch, which is one of the critical issues for bipolar device processing, a unique doping-dependence etch was discovered for InAs that enables the base access etch to stop at the appropriate layer. In other bipolar and HBT-type structures, graded or intermediate etch-stopping layers are introduced to control the access etch to the base layer. Introduction of graded layers and barrier layers, however, alters the carrier transport across the junctions influencing the device performance. In the structures studied here, the etch rate difference between *n* and *p*+ type layers was sufficient to be used as an etch stop criterion. Through interactive molecular beam epitaxy (MBE) growth, device characterization, and material analysis techniques, initial limitations imposed by excessive leakage current of the InAs junctions were addressed and suitable rectifying diodes were produced.

This report is organized as follows. First, the key processing steps, such as ohmic contacts, etching, and their development are summarized. Then the results from the device characterization of samples provided by the University of Rochester (UR) and processed at NRL are discussed. The results from three NRL-grown structures are also discussed. A total of nine UR structures and three NRL structures were processed. Four of the structures processed were intended for bipolar three-terminal devices. The main challenge in having notable three terminal device characteristics was identified as the control of reverse leakage current in the InAs *pn* junctions. The low bandgap InAs and heavy doping resulted in premature breakdown through current tunneling and uncontrollable reverse leakage current. This issue was addressed successfully and *pn* junctions with reverse leakage current as low as 10 μA at –1 V were observed with breakdown voltages as high as 6.5 V. The material structures processed into devices are summarized in Table 1 according to the chronological order in which they were made available for this work.

Manuscript approved May 28, 2002.

Table 1 – Materials Structures Processes

1. UR2454 PN Junction

Thickness (Å)	Material	Doping
500	InAs	Be: 1e19
5000	InAs	NID
Substrate	InAs	

2. UR2455 PN Junction

Thickness (Å)	Material	Doping
5000	InAs	Be: 1e19
5000	InAs	NID
Substrate	InAs	

3. UR2460 NP Junction

Thickness (Å)	Material	Doping
5000	InAs	Si: 1e19
5000	InAs	Be: 4e17
Substrate	InAs	

4. UR2462 Base-Tunneling Emitter

Thickness (Å)	Material	Doping
2000	InAs	Si: 1e19
1000	InAs	NID
35	$Al_{0.6}In_{0.4}As$	NID
50	InAs	NID
5000	InAs	Be:1e19
Substrate	InAs	

5. UR2463 TEBT

Thickness (Å)	Material	Doping
2000	InAs	Si: 1e19
1000	InAs	NID
35	$Al_{0.6}In_{0.4}As$	NID
500	InAs	Be: 1e19
2000	InAs	NID
5000	InAs	Si:1e19
Substrate	InAs	

6. UR2464 P-BJT

Thickness (Å)	Material	Doping
2000	InAs	Si: 1e19
1000	InAs	NID
500	InAs	Be: 1e19
2000	InAs	NID
5000	InAs	Si:1e19
Substrate	InAs	

7. NRL R990825F P-BJT

Thickness (Å)	Material	Doping
2000	InAs	Si: 1e19
1000	InAs	Si:1e17
50	InAs	NID
515	InAs	Be: 1e19
100	InAs	NID
2000	InAs	Si:5e16
5500	InAs	Si:5e18
Substrate	InAs	

8. NRL R990825G SL-HBT

Thickness (Å)	Material	Doping
2000	InAs	Si: 1e19
1000	InAs	Si:1e17
50	InAs	NID
$515\left\{\begin{matrix}12\,\text{ML InAs}\\1\,\text{ML InSb}\end{matrix}\right]\times 13$	InAs/InSb	Be: 1e19
100	InAs	NID
2000	InAs	Si:5e16
5500	InAs	Si:5e18
Substrate	InAs	

9. UR2740 PN Junction

Thickness (Å)	Material	Doping
2,750	InAs	Be: 1e19
300	InAs	Be: 6e18
10,000	InAs	NID (~1e17)
Substrate	InAs	

10. UR2741 PN Junction

Thickness (Å)	Material	Doping
2,750	InAs	Be: 1e19
300	InAs	Be: 6e18
10,000	InAs	Si:6e17
Substrate	InAs	

11. NRL R000823N PN Junction

Thickness (Å)	Material	Doping
5000	InAs	Be: 1e17
5000	InAs	NID
Substrate	InAs	

12. UR2820 PN Junction

Thickness (Å)	Material	Doping
1,000	InAs	Be: 1e19
2,000	InAs	Be: 1e18
15,000	InAs	NID
Substrate	InAs	

2. OHMIC CONTACTS

For high-frequency operation of microelectronic devices the ohmic contacts are of major concern. What is required for bipolar devices is low contact resistance to both *p*- and *n*-type material. Physically, one would like the metal and the semiconductor to have aligning Fermi levels. By doping the semiconductor high, the Fermi level of the semiconductor moves closer to the conduction band for *n*-type doping and closer to the valence band for *p*-type doping. This facilitates either direct transport between the metal and the semiconductor or induces acute band bending in the semiconductor energy gap, facilitating carrier tunneling across the semiconductor/metal interface. Knowledge of the semiconductor bandgap and electron affinity, as well as the metal electron affinity, can guide in selecting appropriate metals for ohmic contacts. Nevertheless, the fact that in InAs the Fermi level is believed to be pinned near the conduction band and in combination with the relatively small bandgap translate to expectations of easier *n*-type than *p*-type ohmic contacts. InAs with electron affinity of 4.54 eV requires a metal with a smaller ionization potential and a small resistivity. In addition, the ohmic metal should not react in a deleterious way with the substrate or the atmosphere.

The metalization scheme that resulted in the best contacts was Ti/Pt/Au. Ti is the first metal conducting the InAs surface. Ti is a robust adhesion layer for subsequent metals; it also has an acceptable work function for metal/InAs contact. Pt is best as a contact to *n*-type InAs with respect to ionization potential and is also providing a barrier for the top Au layer. Au is notorious in penetrating III-V semiconductors and forming alloys with subsequent layers. Nevertheless, Au has one of the smallest metal resistivities and is stable without any atmospheric reactions. Au provides a good bonding surface for further device development and is widely accepted in high-frequency devices.

One of the difficulties with the small energy gap of InAs and the tendency to grow naturally *n*-type at least for most MBE processes, is the lack of insulating properties for test structure and device isolation purposes. Consequently, for device development an underlying *p*-*n* junction isolation scheme was devised. The ohmic contacts were evaluated using transmission line measurements (TLM) on mesa-etched structures with an underlying opposite polarity layer for substrate isolation. The current voltage

characteristics between the top layer and the isolation layer that formed effectively a *pn* junction were evaluated. The reverse leakage current of the *pn* junctions was established and set as a guideline for the current level required for the TLM measurements. Table 1 shows the nominal layers for the University of Rochester MBE-grown test structures designed to help answer key processing questions. Measurements on TLM test structures with Ti/Pt/Au universal ohmic contact to both *n*- and *p*-type InAs resulted in specific contact resistivities as low as 3×10^{-8} and 6×10^{-7} Ω–cm^2 for *n*- and *p*-type InAs, respectively. To our knowledge, the specific contact resistivity established for the InAs ohmic contacts is one of the lowest observed in III-V semiconductors, a very positive asset in bipolar high-speed device operation. Figures 1 and 2 show some of the TLM results.

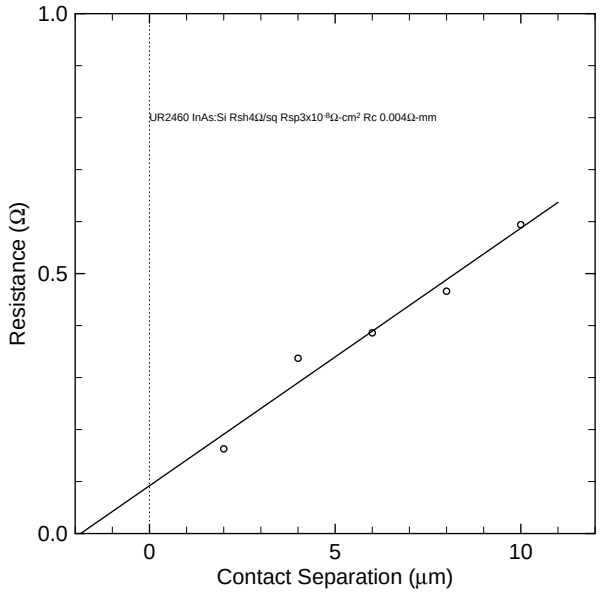

Fig. 1 — TLM measurements of contact resistance for an Si-doped *n*-type InAs layer (5000 Å 2×10^{18})

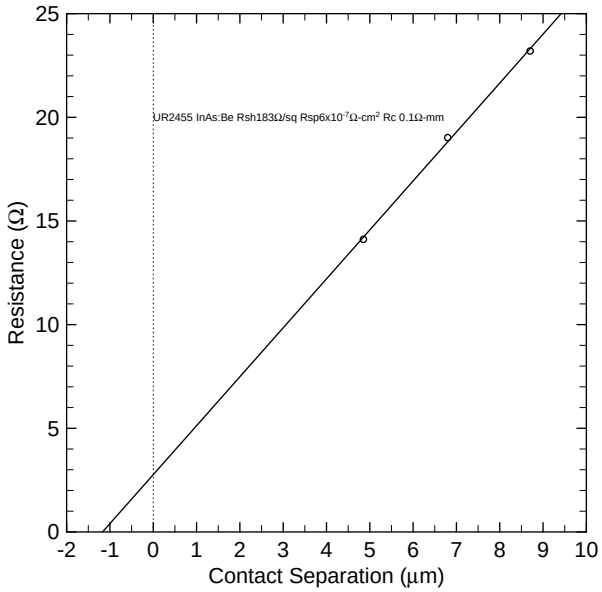

Fig. 2 — TLM measurements of contact resistance for a Be-doped *p*-type InAs layer (5000 Å 2×10^{18})

Annealing the Ti/Pt/Au layers at temperatures ranging from 250 °C to 350 °C resulted in no significant improvement in the specific contact resistivity and raised questions on the integrity of the *pn* junctions. The reverse bias leakage current increases after alloying as it can be seen from the I-V characteristics of Figs. 3 and 4. The I-V characteristics of the same diodes before and after alloying for sample UR2455 with Be-doped top contact layer are shown. The leakage current degradation is evident. Short-like characteristics in *pn* junctions before alloying were encountered in some samples as shown in Fig. 5 for sample UR2460 with Si-doped top contact layer. The high leakage current appears to be location dependent suggesting material uniformity issues. The number of *pn* junctions exhibiting short-like characteristics increased with annealing. The increased leakage current can be attributed to initiation of junction failure mechanism. Excess generation/recombination across the junction eventually leads to junction failure and an ohmic-like behavior. Small bandgap semiconductors are also known to suffer from thermal instability breakdown. The junction temperature increases, either due to actual ambient temperature increase or reverse bias stressing accompanied by an increase in reverse bias current. When the current increases beyond the critical limit, a catastrophic breakdown occurs with permanent linear-like I-V behavior. Physically, the ohmic behavior can also be caused by metal migrating along structural defects through a solid-state diffusion assisted by higher temperatures. Structural defects like dislocations

and vacancies also act as efficient gettering centers attracting metal molecules from the surface. Based on the degradation of the I-V characteristics after alloying, the ohmic contacts were used as deposited without any sintering or alloying.

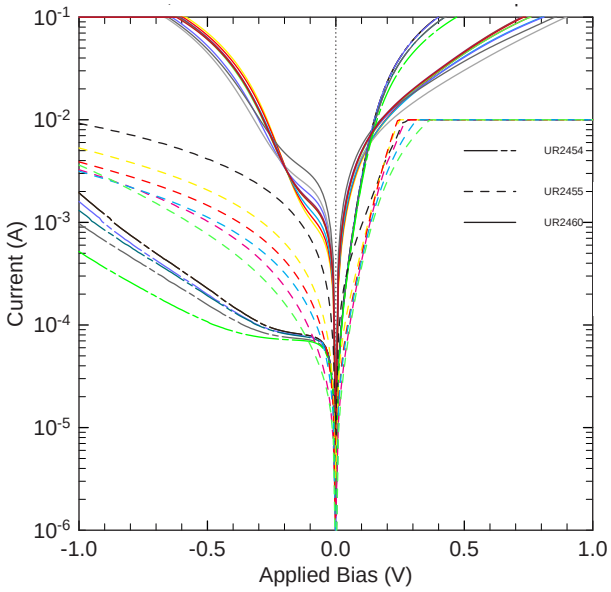

Fig. 3 — *Pn* junction I-V characteristics between the top *p/n* and bottom *n/p* layers of the three ohmic contact evaluation structures

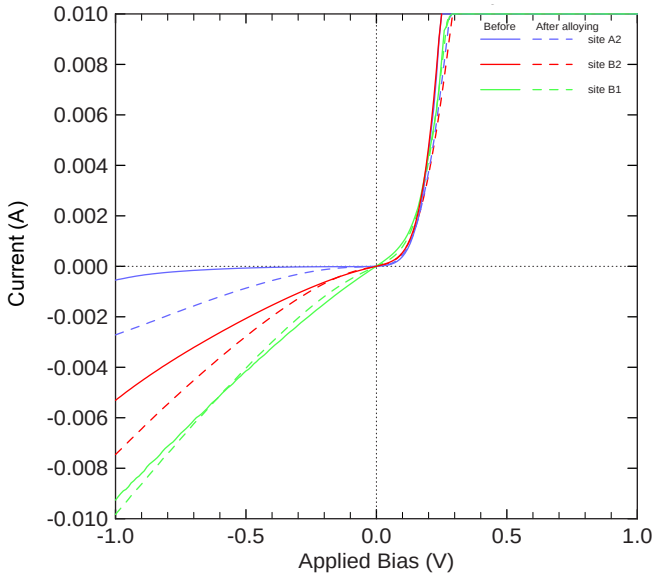

Fig. 4 — I-V characteristics of sample UR2455, InAs *pn* junctions before and after alloying at 250 °C for 60 s

A valuable observation from the ohmic contact and underlying P/N junction characteristics is that the 500 Å Be-doped layer produced good ohmic contacts with no indication of metal penetration beyond the thin layer. This is in fact what is desired for the base metal contact. Figure 3 compares the I-V characteristics from the thin *p*/*n*, thick *p*/*n*, and *n*/*p* structures of samples UR2454, UR2455, and UR2460. The leakage current observed in the thin *p*/*n* junction is comparable with the thick *p*/*n* junction and even lower than the rest. The main result from the electrical characterization is the very high current levels with small bias levels indicative of a potentially high power capability at low voltage levels. Also evident in the above figure is the high reverse leakage current for some of the *pn* structures. What is basically evident is the first grown *pn* junction with only 500 Å of Be-doped layer had significantly less reverse leakage current than any of the subsequently grown structures with thicker Be-doped layers. Cryogenic I-V measurements on the *pn* junctions showed a reduction of the leakage current as expected from the temperature dependence of thermally generated carriers. In one of the structures shown in Fig. 3, negative differential resistance (NDR) was also observed indicative of a carrier tunneling mechanism in action. The cryogenic measurements are further discussed in Device Characterization (Section 5).

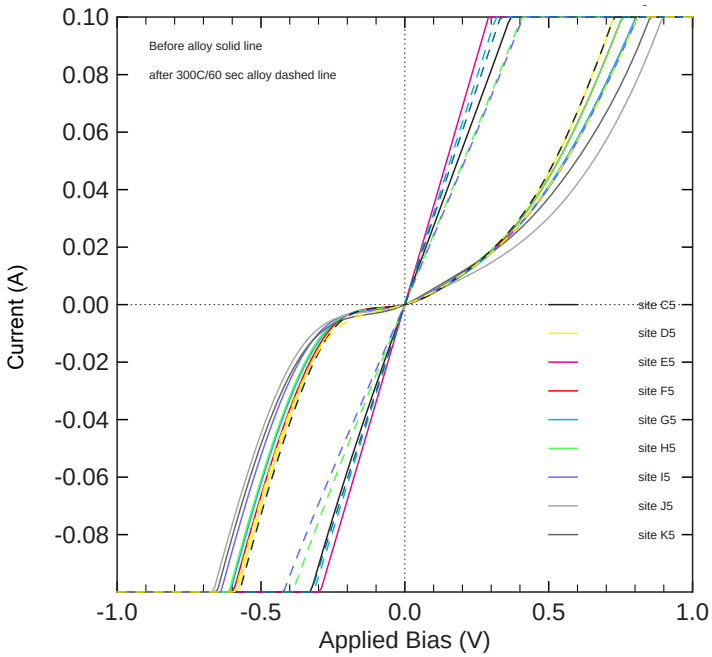

Fig. 5 — I-V characteristics of sample UR2460 *pn* junctions before and after alloying at 300 °C for 60 s. The legend on the right indicates the device location in an x-y side coordinate along the wafer. Note the side dependence on the I-V characteristics.

3. CHEMICAL ETCHING

Low-contact resistance ohmic contacts require a clean semiconductor surface for the deposited metals. The lift-off procedure used a two-layer photoresist process, in which the semiconductor surface is covered with photoresist, which is subsequently developed to expose the semiconductor area where the metal is to be deposited. This semiconductor area will require additional cleaning while preserving the photoresist pattern. Oxygen plasma descumming to remove any possible photoresist residuals was therefore performed. Subsequent chemical etches were applied in order to remove any oxides present on the InAs surface, with an additional requirement of not attacking the photoresist. The surface cleaning procedure prior to metal deposition is a critical process.

A series of possible chemical etches were examined. Figures 6 through 9 show a patterned InAs substrate (UR2455) before and after chemical etching with BOE, HCl, and phosphoric-acid-based mixtures. HCl is believed to etch most of the group III oxides while BOE is believed to etch most of the group V oxides. The HCl etch attacks the photoresist around the edges of the pattern. This implies that it is either etching the InAs surface or an InAs oxide. The fact that HCl penetrates underneath the photoresist suggests that it is most likely etching an original oxide layer present prior to the lithography or oxygen descum steps. The HCl effects on the lithography are more evident when a confirmed InAs etchant is applied after the HCl dip as shown in Figs. 10 through 14. The main outcome of this study was that only diluted BOE could be used as a pre-evaporation etchant. Diluted HCl and BOE can be used as an oxide stripant before the lithography process. The most desirable sequence of etching is BOE first followed by HCl or the etching mixture as evident from Fig. 12. Other acids attacked the InAs surface either too fast (like the phosphoric acid-based etches) or undercut the photoresist (like the HCl). The etch profile is also very important for a base access etch. As shown in Fig. 15, the phosphoric-acid-based etch

gave a very flat profile without any trenches along the edges. Trenches would have been unacceptable for a base access etch as they may isolate the thin base layer from the intended base contact access. The etch rate for this structure was 64 Å/s. It should be noted however that a material- as well as doping-dependent etch rate was evident for small area openings. In particular, the base access etch rate for *p*-type material was significantly slower (~60%) than for the *n*-type material. Due to the limited number of samples available, the possibility of an interface-related retardation of the etch rate could not be eliminated.

Citric-acid-based solutions also resulted in very controllable etch rates without significant undercut. Examination of the NH_4OH:H_20:H_2O-based solutions revealed no detectable etch. Because NH_4OH and other bases are often used in photoresist developing solutions, we did not use the NH_4OH pre-evaporation etch in subsequent processing in order to preserve the small lithographic dimensions of microwave devices.

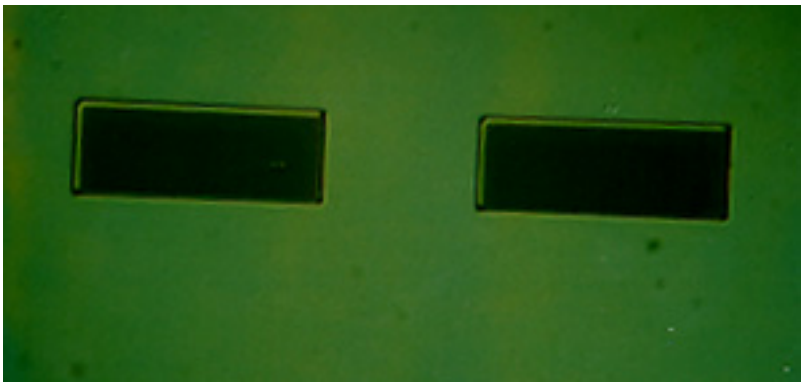

Fig. 6 — Nomarski optical image of photoresist patterned on an InAs sample before any wet chemical etching. (All colors are artificial, resulting from polarization. Magnification is 400X.)

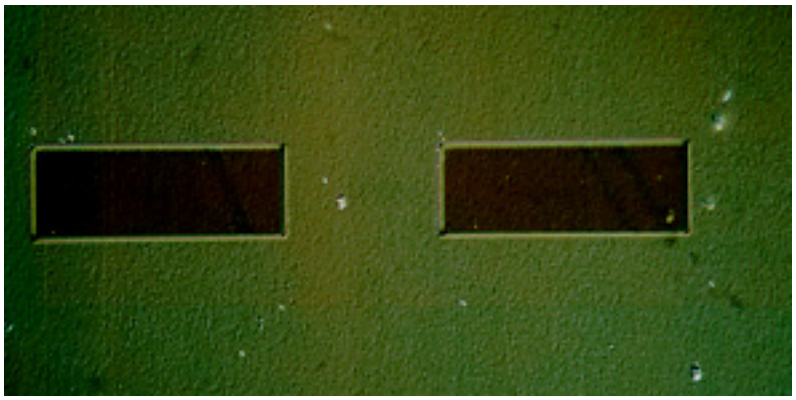

Fig. 7 — Nomarski optical image of photoresist patterned on an InAs sample of UR 2455 after etching in 1BOE:1H_2O for 10 min. No deterioration of the photoresist or etching of the substrate was observed (magnification is 400X).

Fig. 8 — Nomarski optical image of photoresist patterned on an InAs sample of UR2455 after etching in $1HCl:1H_2O$ for 10 min. Deterioration of the photoresist around the pattern is obvious. Although no measurable etching of the substrate was observed, defects appeared to be delineated. (Magnification is 400X.)

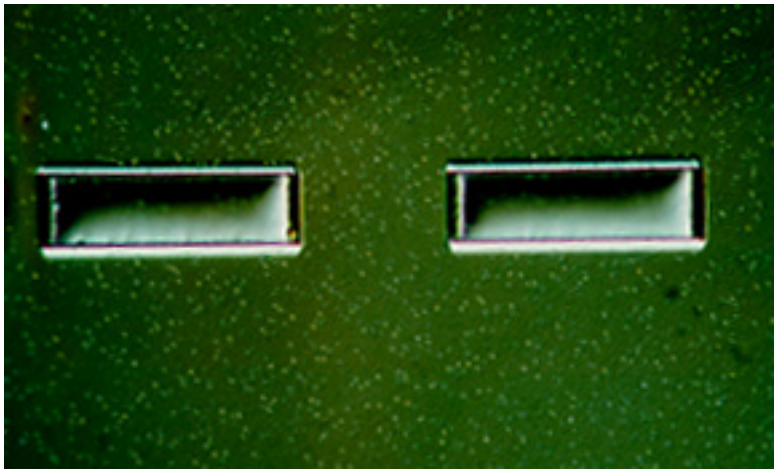

Fig. 9 — Nomarski optical image of photoresist patterned on an InAs sample of UR2455 after etching in $1H_3PO_4:2H_2O_2:20H_2O$ for 10 min. The observed etch rate was 64 Å/s. (Magnification is 400X.)

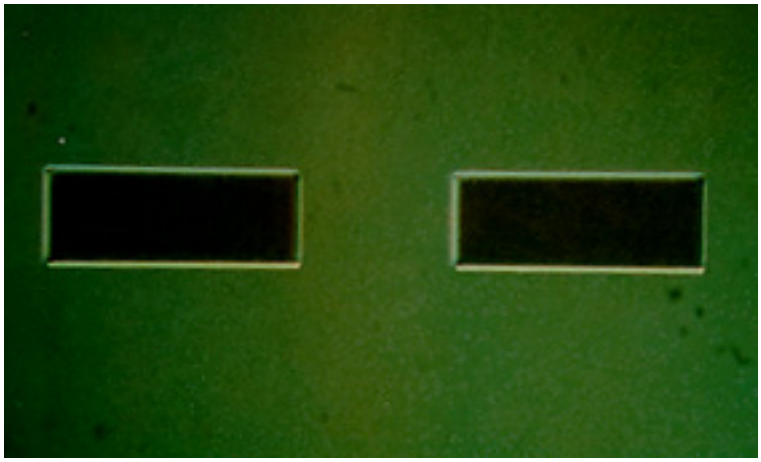

Fig. 10 — Nomarski optical image of photoresist patterned on an InAs sample of UR2455 after etching in $1H_3PO_4$:$2H_2O_2$:$20H_2O$ for 100 s. The observed etch rate was 64 Å/s. (Magnification is 400X.)

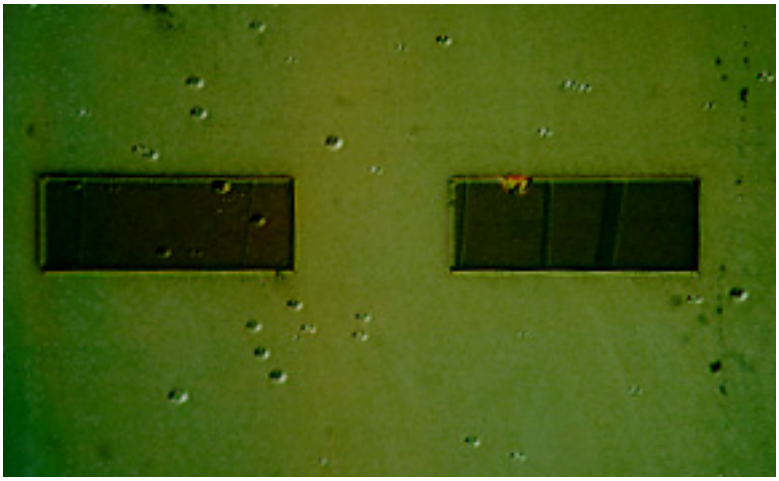

Fig. 11 — Nomarski optical image of photoresist patterned on an InAs sample of UR2455 after etching in 1BOE:H2O for 30 s followed by a DI rinse and a 100-s $1H_3PO_4$:$2H_2O_2$:$20H_2O$ etch. The observed etch rate was 64 Å/s. (Magnification is 400X.)

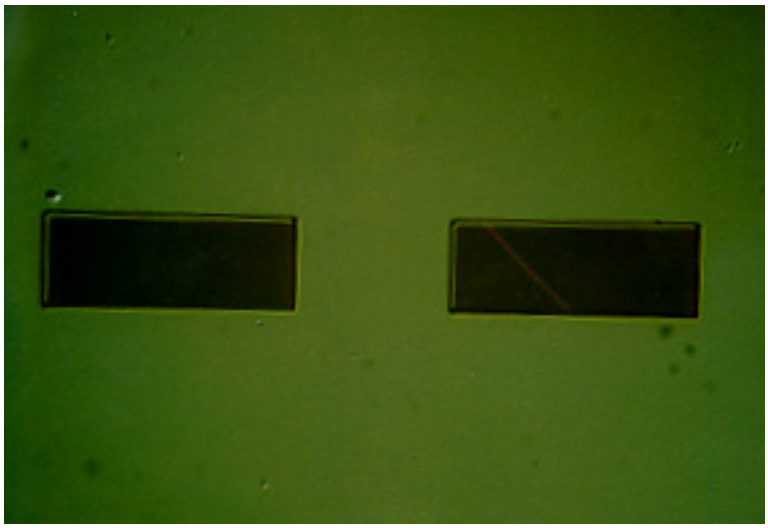

Fig. 12 — Nomarski optical image of photoresist patterned on an InAs sample of UR2455 after etching in 1BOE:H_2O for 30 s followed by a DI rinse and a 30-s 1HCl:1H_2O etch. There was no detectable etch. Notice the clean photoresist edge, suggesting that an etching sequence of BOE followed by HCl is preferable. (Magnification is 400X.)

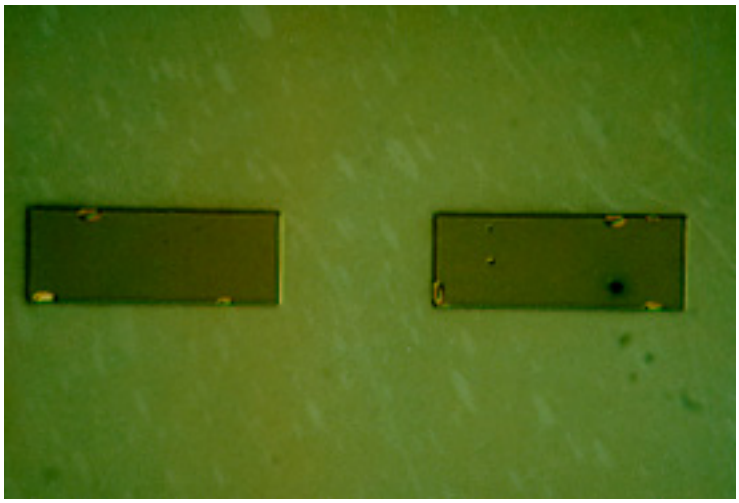

Fig. 13 — Nomarski optical image of photoresist patterned on an InAs sample of UR2455 after etching in 1HCl:H_2O for 30 s followed by a DI rinse and a 100-s 1H_3PO_4:2H_2O_2:20H_2O etch. The etch rate was 64 Å/s. Notice the bubbling along the photoresist edge. (Magnification is 400X.)

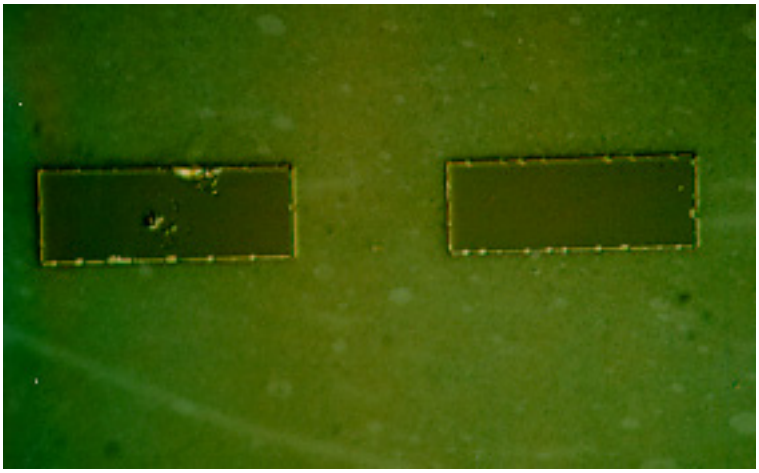

Fig. 14 — Nomarski optical image of photoresist patterned on an InAs sample of UR2455 after etching in 1HCl:H_2O for 30 s followed by a DI rinse, a 30-s 1BOE:1H_2O etch, and a 100-s 1H_3PO_4:2H_2O_2:20H_2O etch. The etch rate was 64 Å/s. Notice the bubbling along the photoresist edge. (Magnification is 400X.)

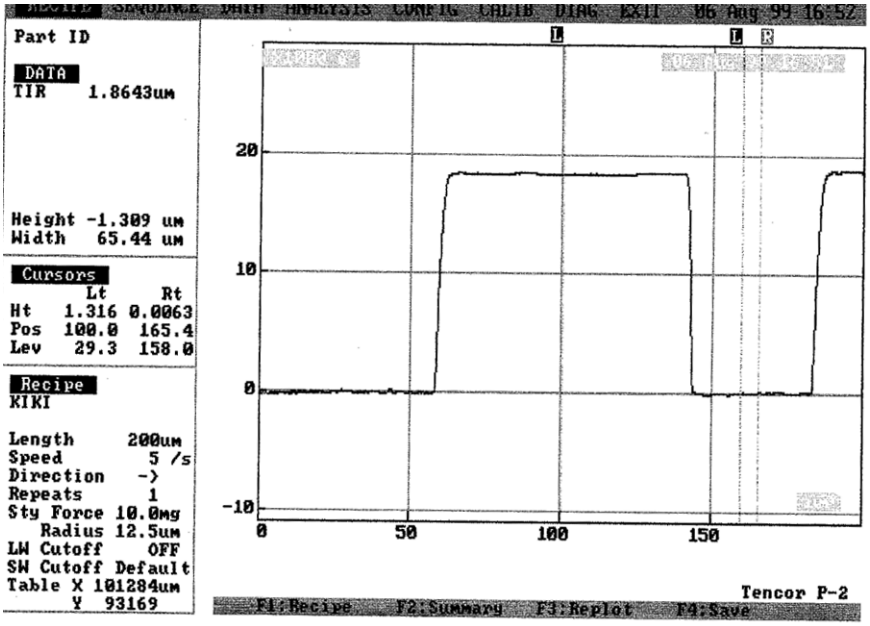

Fig. 15 — Profilometer traces of a phosphoric-acid-based etch of the sample shown in Fig. 14. Notice that a very desirable flat profile without any trenches is obtained. Trenches along the patterned edges would have been unacceptable for a base access etch of a bipolar structure. Photoresist is still on for this trace.

4. DEVICE FABRICATION PROCESS

A mesa-etch device fabrication process was adapted. The emitter base and collector were defined using successive mesa etches to access the respective layers. The critical issues of the mesa-etch process are the accuracy of the etch in allowing reliable access to the subsequent layers and in undercut control to achieve the minimum desired dimensions. In both cases, material quality influences both etch rates and undercut. Consequently, the major part of the device processing development was the identification of suitable etches for the MBE TEBT structures. Some of the chemical etch is described in Section 3. InAs etches as nicely in citric-acid-based solutions as in phosphoric acid. An etch rate reduction was observed when reaching the highly Be-doped base layers. The etch-rate differential was particularly enhanced when accessing the base by etching through small windows. The size dependence is an indication of a diffusion-limited etch rate. The reduced etch rate was used as an indication to terminate the etching process when accessing the base layer. For the InAlAs tunneling emitter, no significant etch rate reduction was observed for the etches tested. For the InSb superlattice base structure, the base etch rate for both the phosphoric- and citric-acid-based etches was higher than in the layers without Sb. All the metal delineation processes were performed with a double-layer PMGI/photoresist process. The double-layer process provided an adequate T-shaped profile for sharp metal edges, necessary for high-frequency devices.

Table 2 shows a sequence of the fabrication process. The base access etch, being the most critical, was performed first. The subcollector mesa etch will be incorporated in future RF devices for structures grown on semi-insulating (SI) substrates or transferred to SI substrates. The interlevel isolation devices were made of low-temperature, plasma-enhanced, chemical-vapor-deposited Si_3N_4. Second-level metalization can be Ti/Au. Figures 16 and 17 show optical microscope images of large area bipolar transistor structures on samples of UR2463 and NRL R990825F P-BJT, respectively. After the identification of the Ti/Pt/Au as a universal *n*- or *p*-type metalization for InAs, a new mask set for fast material evaluation was developed and shown in Table 3. The emitter metal in that case is used as the masking material for etching to the base. The base etch was followed by a collector access etch and a single base/collector metalization.

Table 2 — Photolithography Mask Levels and Processing Sequence

1	Base access etch
2	Collector access etch
3	Subcollector mesa etch
4	Base metalization
5	Emitter/collector metalization
7	Dielectric via etch
7	Second-level metal

Table 3 — Fast Process Sequence
for Material Evaluation

1	Emitter Metalization
2	Base Access Etch
3	Collector Access Etch
4	Base/Collector Metalization

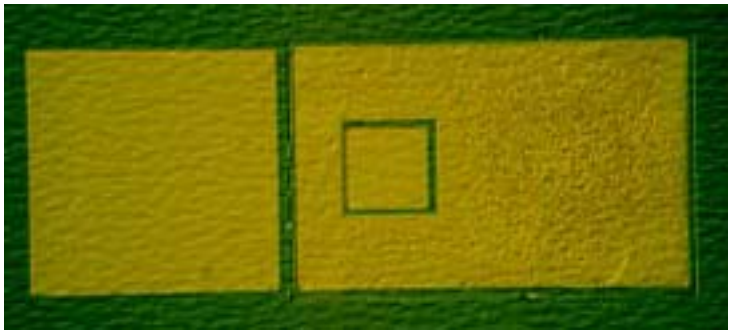

Fig. 16 — Large area bipolar transistor fabricated on a sample of UR2463. Emitter is the small square in the center, surrounded by the base. The base etch is slightly rougher due to the high doping-related slower etch rate that was used as an etch-stopping criterion. The collector metal contact is the large square structure on the left. Also notice the rougher surface morphology of this InAs sample. (Magnification is 400X.)

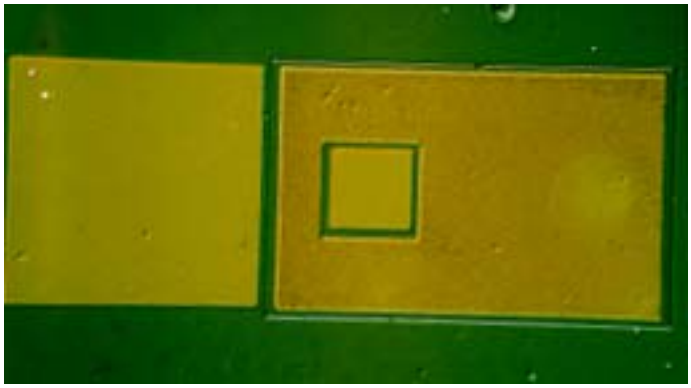

Fig. 17 — Large-area bipolar transistor fabricated on a sample of NRL R990825F P-BJT. Notice the smoother InAs surface morphology of this sample. (Magnification is 400X.)

5. DEVICE CHARACTERIZATION

The characteristics of the processed devices are described in this section according to the chronological order in which the structures were received and processed. In brief, the first batch of samples appeared to suffer from excess leakage current. Cryogenic measurements and secondary ion mass spectroscopy (SIMS) profiles helped identify the origin of the excess leakage as being the high background *n*-type doping. Highly doped layers are prone to tunneling-assisted breakdown through band-to-band recombination. The bipolar structures suffered from excessive Be redistribution around the base layer and premature breakdown at the base/collector junction. The Be redistribution was also identified in the SIMS profiles. The base/collector premature breakdown is believed to be related to the excess high doping of the initial structures and to charges from the interface between the substrate and the MBE-grown layers. Subsequent structures were designed to address the excess leakage current issue and are listed in Table 1. Basically the growth temperatures were tailored to reduce the dopant redistribution's and the background doping in NID layers controlled. The buffer layer was also grown significantly thicker to reduce the charges from the interface.

Structure UR2462 was a first attempt of the emitter/base tunneling junction. Unfortunately, it appeared to have some difficulties. Figure 18 shows some of the characteristics obtained. The sample was cloudy and white in color at the edges. There was a high defect density, giving it a rough growth look under the microscope. I-V characteristics of large area devices did not exhibit any rectification. Some of the large-area devices had a slight asymmetry in their I-Vs but it was hard to identify this as rectification or as *pn* junction-like behavior. Devices closer to the original central area of the wafer appeared to have *p/n* junction characteristics that were less linear. Very small-area devices (three-finger microwave bipolar transistors) after testing had asymmetric I-Vs, which might be what one would expect from the E/B junction effect. Nevertheless, it should be noted that as in all the InAs devices tested here, the junctions become ohmic at 0.3 V. The voltage of operation is very small, which is desirable for low power dissipation and is as expected from a narrow bandgap material. However, since thermal generation covers desired effects at room temperature, we pursued a low-temperature characterization. Also, for the UR2462a sample with an additional etch and metalization, we contacted the InAs:Si doped substrate, which acted as a collector layer. Figure 19 compares small area, large area, and emitter and base TLM ohmic structures on the E/B UR2462 structure. The fact that small-area devices without visible defects had less leakage might suggest a defect-related enhanced leakage.

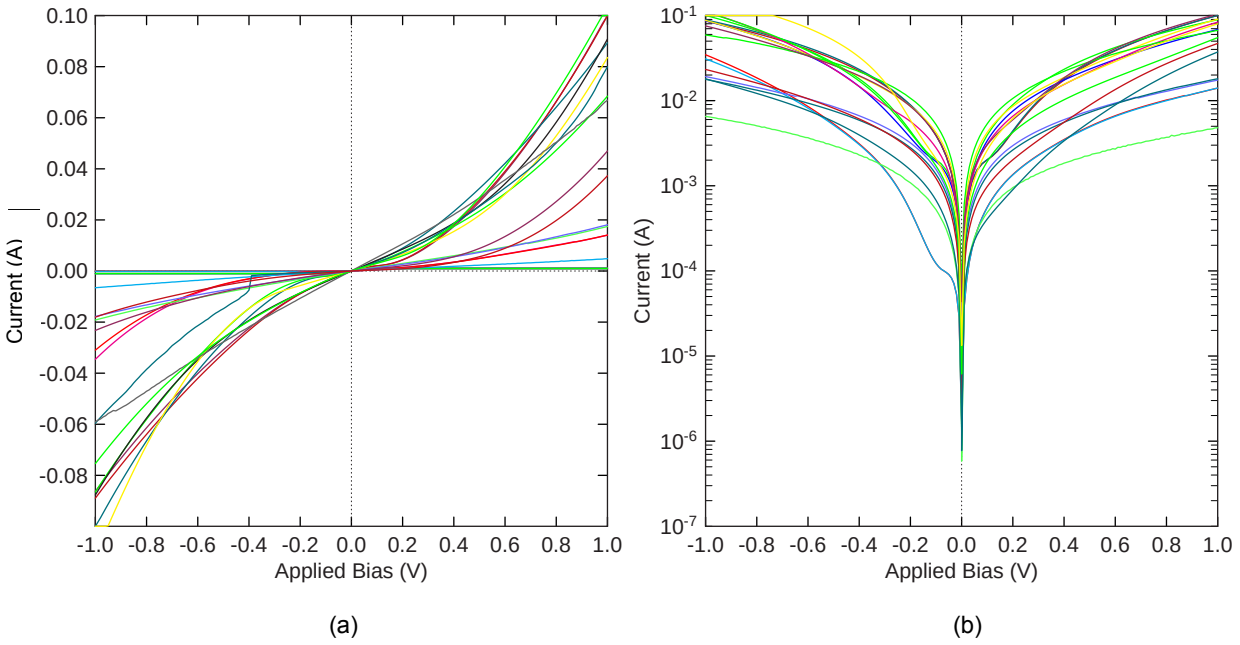

Fig. 18 — E/B junction characteristics of structure UR2462 ((a) linear and (b) log scale). It consists of a 2000 Å InAs:Si 1e19, emitter contact, 1000 Å InAs NID Emitter, 35 Å tunneling layer, 50 Å InAs (NID) diffusion retardation layer, and 5000 Å InAs:Be 1e19 *p*-type baselike layer. Different lines correspond to different devices across the sample.

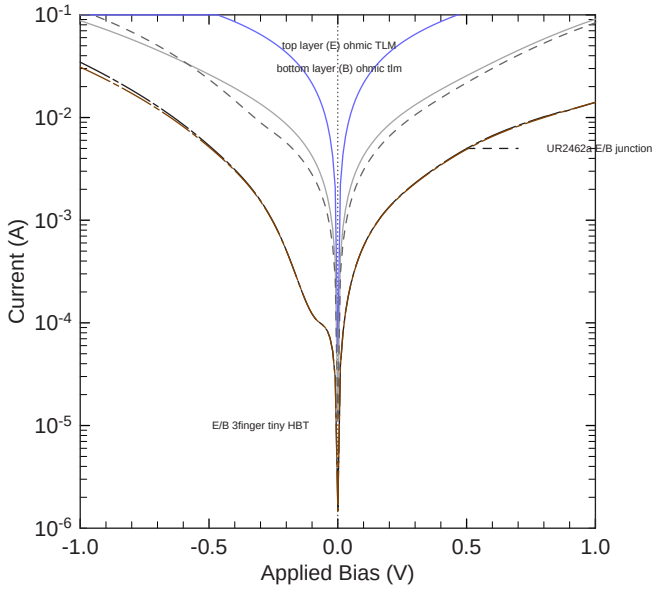

Fig. 19 — UR2462a E/B junction characteristics of a large- and small-area device in comparison with the ohmic emitter and base contacts

The surface morphology for the TEBT structure UR 2463 was better than the E/B UR 2462 structure. There was a location dependence with leaky I-Vs becoming more leaky moving towards the periphery of the sample. Some rectification features were observed below 0.4 V but become very ohmic after 0.6 V.

When comparing the TEBT with the P-BJT UR2464 structure, the P-BJT structure without the AlInAs barrier layer appears to have better defined rectification (back-to-back diode). This might imply that the tunneling barrier or the doping layers are intermixing in the TEBT structure. Figure 20 shows a number of I-Vs from the emitter /collector junctions of the TEBT and P-BJT structures.

The NRL-grown InAs samples R990825F and G had fewer structural defects and different morphology than the UR InAs samples. The NRL samples were apparently grown on thinner InAs substrates than the UR samples and were extremely fragile. Some slight rectification is evident but characteristics appear extremely leaky. The P-BJT structure has more features and lower leakage current below 0.3 V. Figure 21 plots the I-V characteristics of both NRL-grown samples.

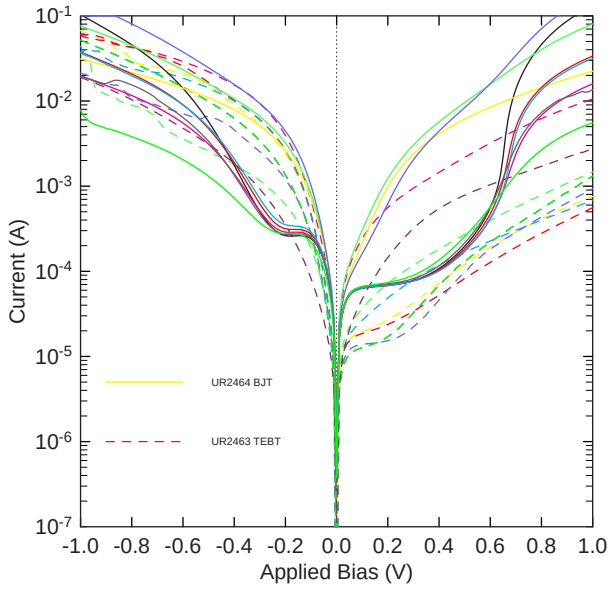

Fig. 20 — I-V characteristics of E/C junctions of UR2463a TEBT and UR2464a P-BJT structures

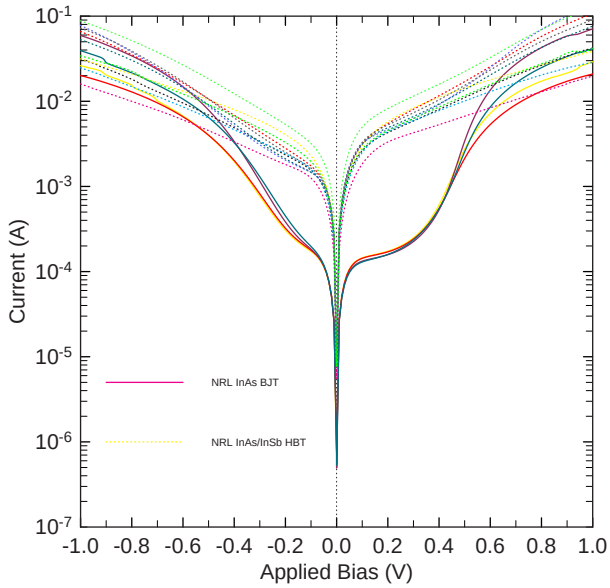

Fig. 21 — E/C I-V characteristics of NRL-grown samples R990825G and F. The different traces are from different devices across the sample.

In comparing the two P-BJT structures in Fig. 22, we can see that they appear very similar, with the UR BJTs tested having slightly lower current levels. The expected I-Vs would be similar to a back-to-back diode. In practice, however, we have two different diodes. The collector contact is the whole sample while the emitter is only the top of the etched mesa. From simple area considerations, the base emitter junction is smaller than the base collector junction, leading to asymmetric diode characteristics.

In comparing selected devices from the UR TEBT and NRL HBT in Fig. 23, it appears that the AlInAs TEBT structures tested might have a more effective barrier than the InAs/InSb superlattice base structure. Nevertheless, it should be stressed that any conclusion is rather premature. Both of these structures are the first try. TEM cross-section results indicate interfacial problems and improvements can be made in subsequent growths and device processing.

The bipolar structures, a TEBT and a pseudo-HBT structure grown by UR and a similar pseudo-HBT with a SL-InAs/InSb base HBT structure grown by NRL, were processed into three-terminal devices. However, three-terminal device characteristics were only observed at cryogenic temperatures. The current gain was very small with insufficiently saturating characteristics. An example of the marginal bipolar action at 17 K is shown in Fig. 24. Although not the desired saturating current characteristics, the current gain at low bias is about 10 but at high bias is over 80. The main difficulty was identified as high current levels in the base collector junction. The base collector junction would prematurely break down after an initial short-lived junction-like behavior. Subsequent efforts were focused in further studying the respective structures in order to identify the MBE layer structure changes required to obtain the desired results.

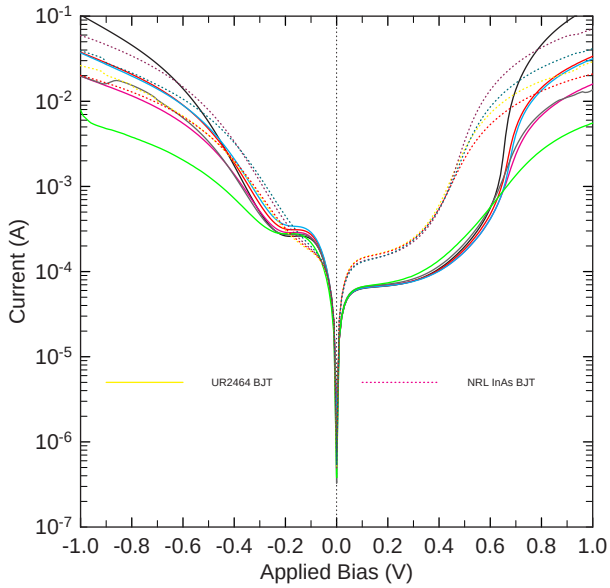

Fig. 22 — A comparison of the I-V characteristics of the two P-BJT structures. The different traces are for different devices across the sample.

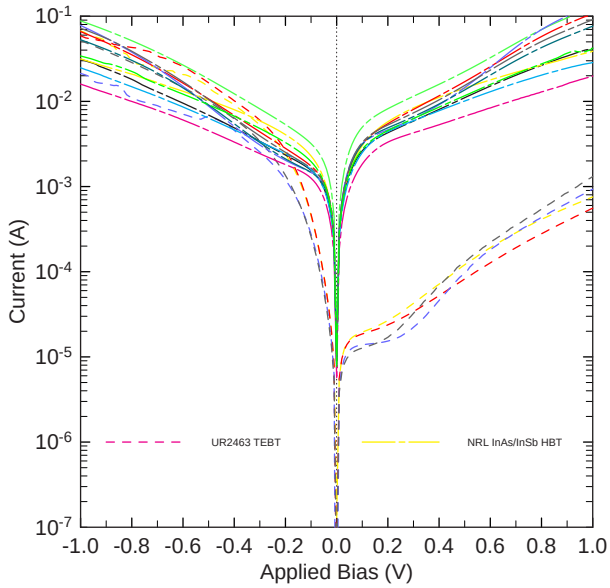

Fig. 23 — A comparison of the I/V characteristics of E/C junctions of the HBT and TEBT structures

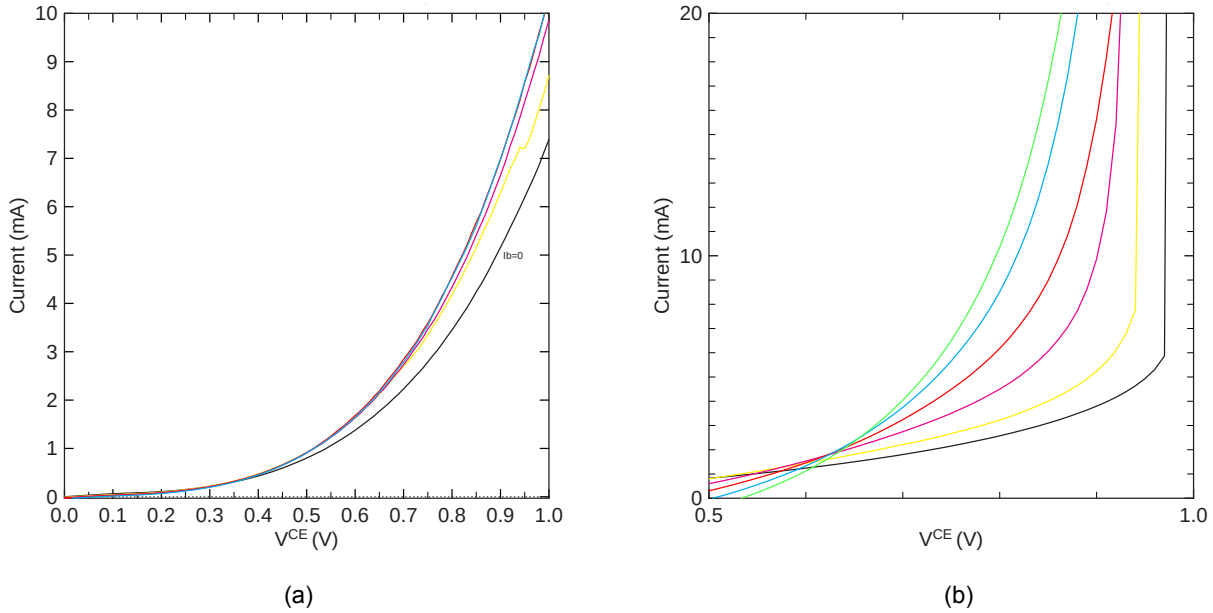

Fig. 24 — Examples of the I-V characteristics obtained at 17 K for the tested transistors: (a) UR2464a with a base current step at 1×10^{-5} A, and (b) NRL R990825G with a base current step at 5×10^{-4} A. The current gain ranges from 2 to over 100 but the characteristics do not exhibit the desired saturation region at high biases due to excessively high leakage currents, leading to a premature junction breakdown.

5.1 Cryogenic Measurements

Cryogenic characterization of the InAs *p/n* junctions was very informative in identifying the possible origin of the high leakage current. Figures 25 through 28 show some of the cryogenic I-V characteristics obtained. Sample UR2524 was particularly useful since its relatively lower leakage currents allowed the observation of negative differential resistance (NDR) at low temperatures, suggesting a tunneling mechanism is in action. The low peak voltage agrees well with what is expected from band-to-band tunneling in InAs. At higher temperatures, the thermal carrier generation is such that the tunneling current is masked under a slight wiggle in the I-V characteristics.

5.2 SIMS Analysis

SIMS analysis of the InAs structures was performed by Evans East, Inc. and revealed significant out-diffusion of Be. The superlattice InSb/InAs structure had a better confined Be layer. Some of the SIMS results are shown in Fig. 29; the corresponding nominal structures are listed in Table 1. For the InAlAs TEBT, the Be from the base layer extended into the tunneling emitter layer, compromising the expected carrier transport. For the pseudo-HBT structures that depend on bandgap narrowing in a highly doped base, the spreading of Be does not support a high enough localized concentration for the necessary bandgap narrowing. In addition, the high background doping of the *n*-type InAs results in an unintentional bandgap narrowing effect in the emitter and collector layer bandgap. Figure 30 shows that the expected effective bandgap for a *p*-type 1e19 InAs and *n*-type 1e17 InAs layer at room temperature is 0.311 eV and 0.332 eV, respectively. In comparison with the expected low doped room temperature Eg of InAs of 0.36 eV, the small energy differential from bandgap narrowing can be easily overcome by the thermal energy kT/q. Consequently, for the pseudo-HBT, which depends on bandgap narrowing in the base only to achieve a functioning device, a lower background *n*-type InAs and a higher doped, well-confined, and

localized Be- doped layer have to be achieved. In addition, the SIMS results indicate that the UID layers were high in C and O, both suspected of being *n*-type-like dopants in InAs.

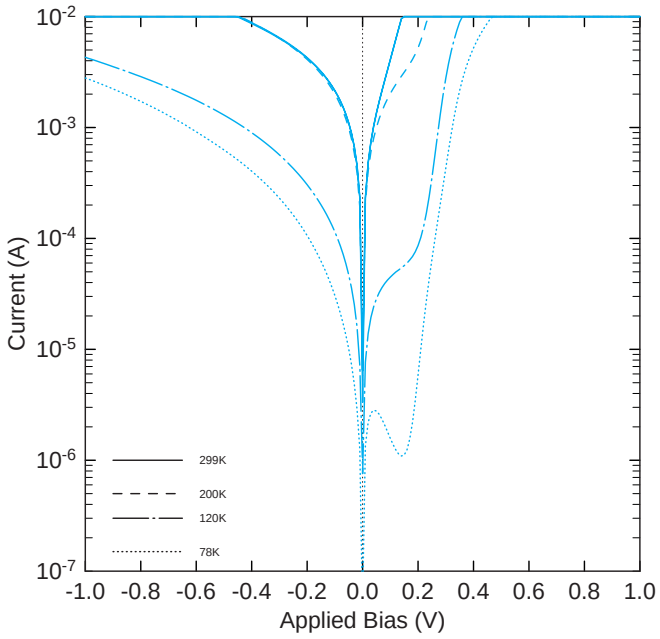

Fig. 25 — Cryogenic I-V characteristics of UR2454 InAs *pn* junction, device E3, showing NDR at 78K

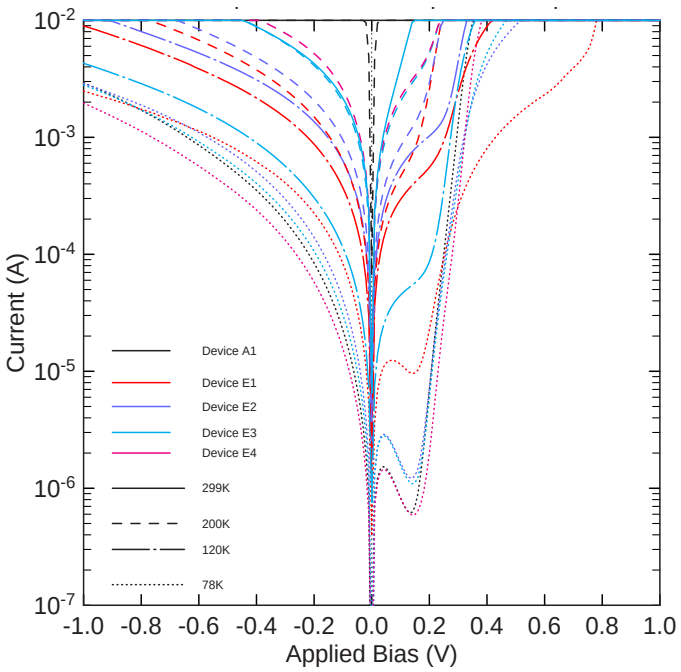

Fig. 26 — Cryogenic I-V characteristics of UR2454 InAs *pn* junctions across the sample. All devices exhibit the NDR characteristics at 78 K. There is some location dependence on the current levels observed.

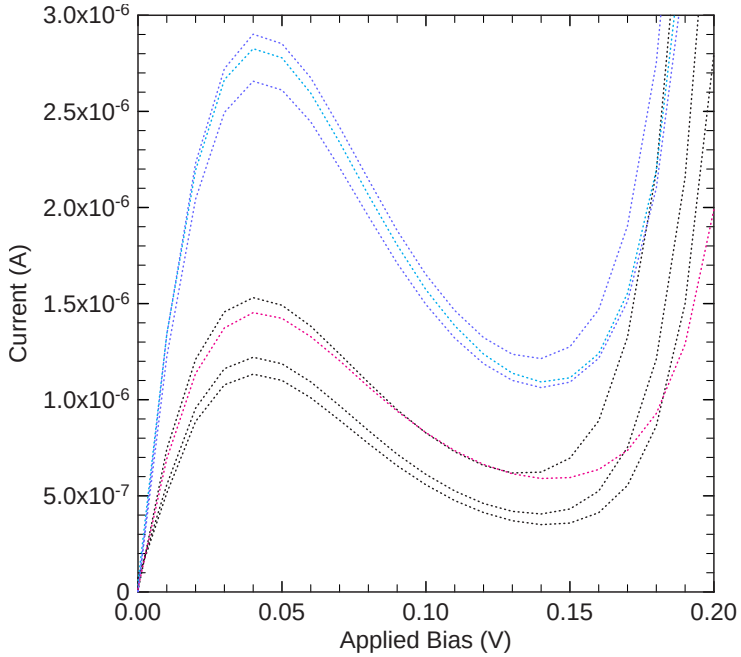

Fig. 27 — I-V characteristics of UR2454 for InAs *p/n* junctions at 78 K. The different color curves correspond to different devices as specified in the legend of the previous figure. The peak and valley voltage levels occur at about 0.04 V and 0.014 V, respectively, for the devices tested.

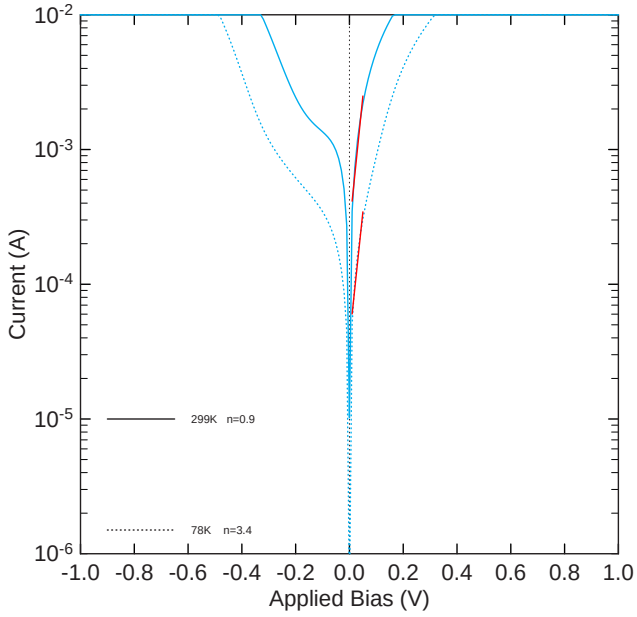

Fig. 28 — I-V characteristics and ideality factors at RT and 78 K for *p/n* junction UR2460. Although forward-bias ideality factors at low biases are close to unity, the excessive reverse bias leakage current persists even at low temperatures.

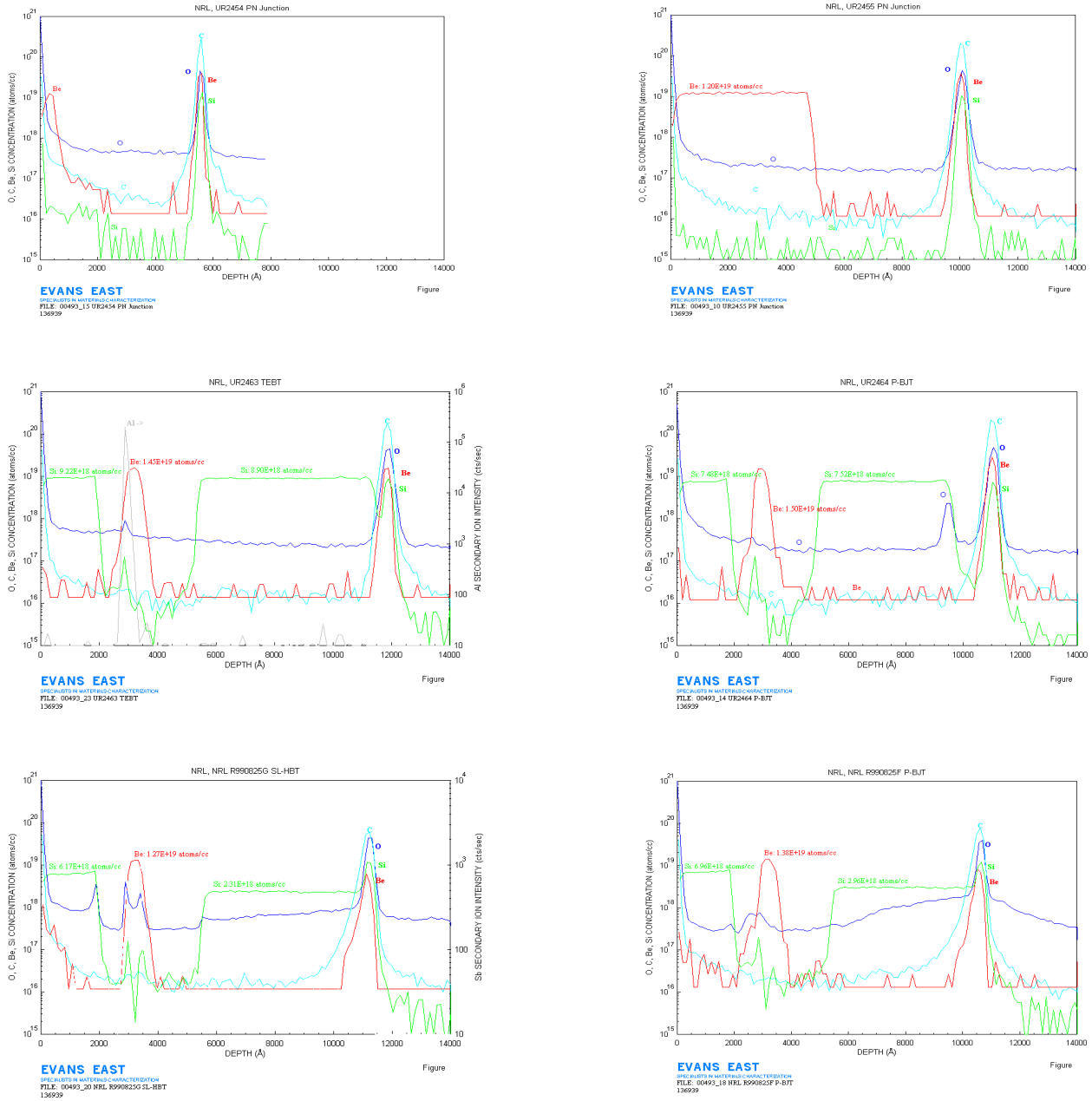

Fig. 29 — SIMS analysis profiles for some of the InAs bipolar structures studied here. The nominal structure layers are listed in Table 1.

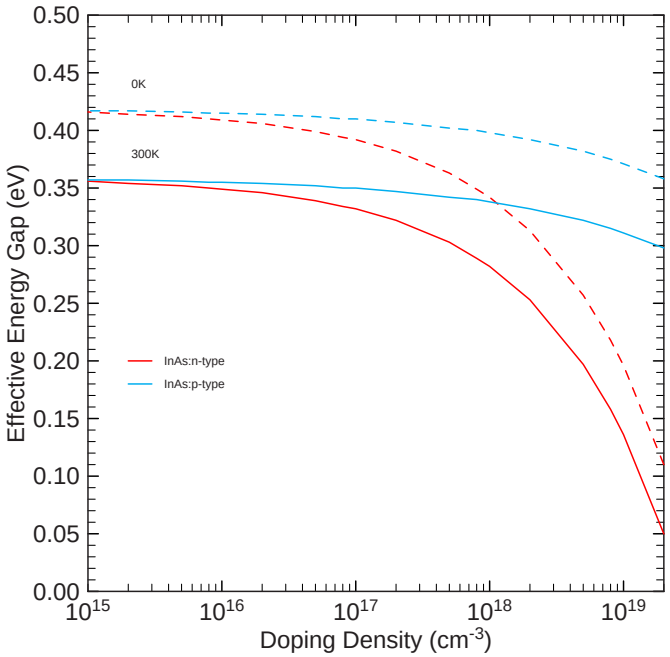

Fig. 30 — Expected bandgap narrowing in InAs calculated using the Jain-Roulston formulation [5-6]

One of the concerns was the identity of the unintentionally background *n*-dopant that resulted in some cases to a background *n*-type doping of 1-7 × 10^{17} cm^{-3}. One would expect oxygen (O), sulfur (S), selenium (Se), and tellurium (Te) to be *n*-type dopants from Group VI simple electronegativity arguments. Se, Sn, Te, and S have been used as *n*-type dopants for InAs. H_2S is used to dope InAs MOCVD with S for *n*-type. Additional SIMS analysis for other InAs test samples, like UR2616, indicates high S concentration on the bulk and surface. It appears that the substrate must be S-doped InAs. It is possible that some autodoping from the substrate occurred, causing the high S surface measurement. As for the rest, C, although potentially amphoteric, is believed to be an *n*-type dopant for InAs. This is attributed to the weak In-C bond [1]. C tends to replace the III group, resulting in an extra electron for *n*-type doping. Also monovacancy impurity complexes in InAs are related to *n*-type doping in the 7 × 10^{16} to 1 × 10^{17} level [2].

The closest to InAs:O donor possibility comes from Furukawa and Ideshita [3]. They discuss oxygen in InAs/AlSb QW that is MBE grown. They measured by SIMS oxygen levels in the 3-8 × 10^{17} cm^{-3} range. They attribute the donor density in the QW to oxygen in the AlSb. They also identified the origin of the unintentional O dopant as being the Sb MBE source. It is interesting to note that they see the same oxygen accumulation in interfaces during growth interruption as in the NRL SIMS sample. Unfortunately, Furukawa and Ideshita were trying to identify the InAs/AlSb QW donor source by doing all the SIMS studies in the AlSb layers and in AlSb/GaSb — that is, they did not investigate the possibility that oxygen is a direct donor to InAs as well as to AlSb. They assumed that the O in the AlSb, acting as a deep electron donor, is causing the modulation doping effect in the InAs wells of the QW and the corresponding effective electron density.

Also, earlier MBE papers refer to the oxygen donor possibility [4]. They report improved electrical properties using a different arsenic source that did not oxidize. They also mentioned supportive evidence from degrading InAs grown layers under high oxygen gaseous conditions. In addition, the residual electron concentration was reported to be between 5×10^{16} and 2×10^{18}. High growth rates and In and As^4 fluxes produced higher residual *n*-type concentrations. The high As fluxes were suspected of causing the *n*-type doping and Grange et al. speculated that As was either incorporated as an As^4 inclusion within the epi-layer, or caused In vacancies in the grown layer [4].

Oxygen, either substitutional or in a complex form, is a very legitimate prime suspect for the background *n*-type in InAs. To the best of my knowledge to this day, no published control studies exist for InAs:O. It would be preferable to be able to control the *n*-type for our devices in order to establish a low background doping. The intrinsic carrier concentration for InAs at 300 K is 9.2×10^{14} cm^{-3}, so we can theoretically achieve lower background levels than the 10^{17} cm^{-3} we have seen.

5.3 Layer Troubleshooting

The SIMS analysis also shows the nominal layer thickness being thinner than expected, making relying on nominal structure specifications for device fabrication a high risk process. Subsequent processing experiments focused on finding room temperature observable electrical characteristics or etch stop properties that will facilitate device processing.

Figure 31 shows the results for one of these experiments. In particular, the TLM pattern was used. The current voltage characteristics between two ohmic contacts separated by 50 μm was monitored as the etching proceeded in a slow sequential manner. A high-resolution step profilometer and the SIMS analysis results were used to identify the exact location of the layers involved. The theory behind this approach is that as the material between the pads is etched away, the current will be spatially forced to flow through the exposed layer. Consequently, at the beginning, before any etching is done, the two ohmic metal pads' I-V is the expected straight-line resistance. As the material between the pads is etched away, current is forced through the lower layers. As the *p/n* junction is encountered, the current flow I-V characteristics between the pads become a back-to-back diode. The I-V characteristics for Fig. 31 are for device R990825G but similar breakdown characteristics at the collector layers were obtained for the UR samples. Both NRL and UR SIMS results indicate an unusual accumulation of unintentional dopants across the MBE layers/substrate interface. This can be traced back to the same InAs "MBE-ready" substrate. Consequently, it appears that the charge accumulated at the interface might be responsible for the low base-collector breakdown voltage observed that inhibited high gain three-terminal device operation. A fast solution for this would be to incorporate a thicker collector or a buffer layer, allowing for some spatial separation between the interface charge layer and the base/collector junction. In fact, as shown in subsequent sections, a thicker collector finally resulted in very well behaved I-Vs for the last samples.

	R980825G	HBT	Be: 2800-3800	Sb 3000-3600								
			Si:0-1800,5800-10600									
	I piece try					New solution						
	original Ti/Pt/Metal	10 sec etch	+20 sec etch	+20 sec etch	+20 sec etch	+20 sec No HCl	+22 sec	+20 sec etch	+40 sec etch	+40 sec etch	+50 sec etch	
	3385	3825	5125	6000	7050	7355	8020	8505	10270	11650	13550	
	3395	3915	5145	5995	6990	7290	8115	8985	10380	11710	13750	
	3385	3830	5100	6060	7095	7445	8080	8985	10770	12040	14300	
		3920	5165	5980	7045	6905	8105	8785	10560	12100	14110	
						7375						
average	3388	3873	5134	6009	7045	7249	8080	8815	10493	11875	13928	
etch debth		485	1261	875	1036	204	831	735	1678	1382	2053	
etch rate		48.5	63.1	43.8	51.8	10.2	37.8	36.8	42	34.6	51.3	
total etch debth			1746	2621	3657	3861	4692	5427	7105	8487	10540	
total etch rate			58.2	52.42	52.2	42.9	41.9	41.1	41.3	40	40.2	
new solution total etch rate							37.8	37.3	39.6	37.9	38.8	
SIMS profile material ID		n+ InAs	n+ InAs	n-InAs	InAs/InSb SL p+	InAs p+	InAs n-	InAs n-	InAs n+	InAs n+	InAs n+	InAs sub
diode on (rev-break-down)	R 3 Ohms0.15V@50mA	R 3.5 Ohms 0.18V@50mA		Vbd 1V @ 50 mA	Vbd 1V @ 50 mA	Vbd 0.5V@50mA	Vbd 0.7V@50mA	Vbd 0.6V@50mA	Vbd 0.6V@ 50mA	Vbd0.3V@50mA	Vbd 0.3V@50mA	

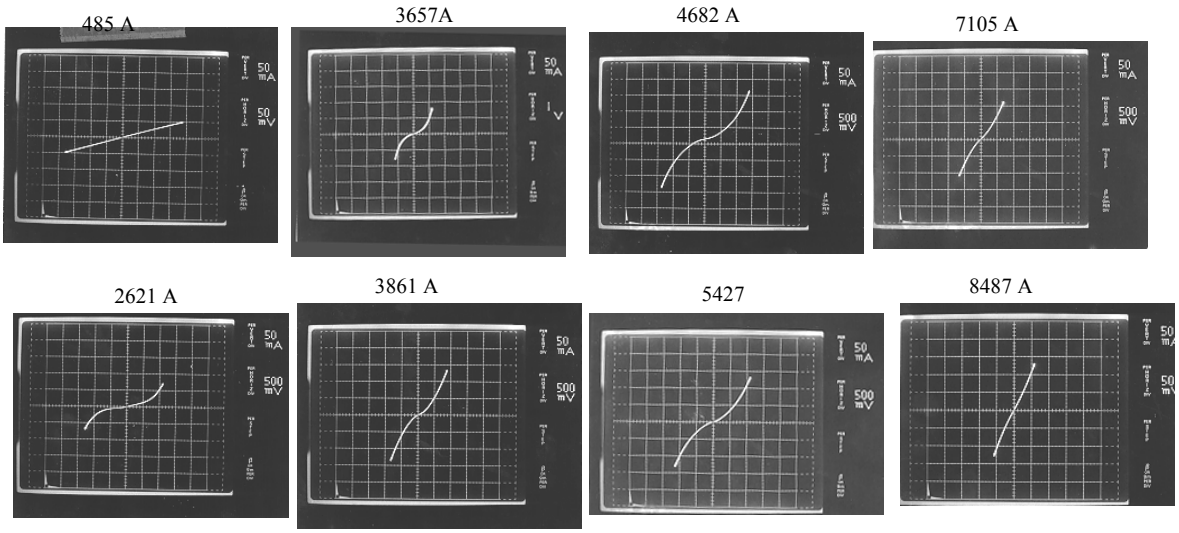

Fig. 31 — I-V results of ohmic contacts as the material between the ohmics is etched away and the current is forced through the under laying *pn* junctions. The initial ohmic contact through the top emitter contact layer turns into a back-to-back diode characteristic after the emitter base junction is encountered. The back-to-back diode characteristics turn ohmic when the current is forced through the base collector junction. Similar behavior was observed in all the three-terminal structures with the base collector junction having nonsustaining reverse bias characteristics. The high NID *n*-type conductivity and high charge from the substrate is believed to be mainly responsible for this effect. Subsequent diodes grown by the University of Rochester team successfully addressed this by controlling the NID doping and by having a significantly thicker buffer layer.

5.4 The Next Generation Attempts

Based on the combined electrical and SIMS analytical results, two additional InAs *pn* junctions were grown in an effort to identify the origin and control the reverse current generation. The new InAs *pn* junctions were of identical Be-doped caps but with NID and Si-doped buffer layers, respectively. Both of the structures indicate higher than desired reverse leakage currents and an undisputed forward bias NDR at high current levels, as shown in Fig. 32. NDR is a characteristic of tunneling effects. Due to the small bandgap of the InAs layer and the high NID background doping levels of unidentified impurities, it is possible that the NDR and high leakage current originate in band-to-band tunneling from degenerated levels across the junction. These tunneling energy levels could also be associated with doping complexes or structural defects, or could be a fundamental material property. Although the observed NDR has numerous potential applications in our device effort, it clearly needs to be addressed and controlled in subsequent work.

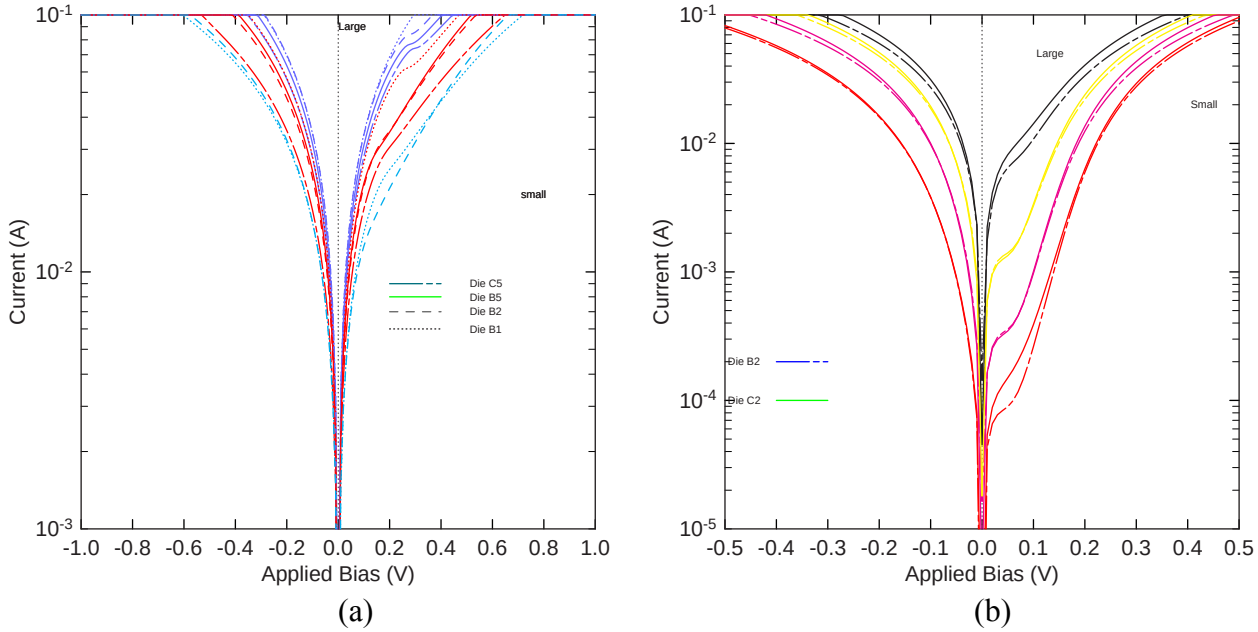

Fig. 32 — Room temperature I-V characteristics of *pn* junctions from samples (a) 2740 (NID *n* layer) and (b) 2741(Si-doped *n* layer)

Sample R000823N with nominal layers of 5000 Å InAs:Be 10^{17} on top of 5000 Å InAs:NID on an *n*-type InAs substrate was processed for *pn* junction evaluation. Earlier results from the UR InAs *p/n* junction samples like UR2740 and UR2741 suggested that heavily doped layers in InAs had very high reverse leakage current, exhibiting weak rectifying junction characteristics presumably due to band-to-band tunneling. Consequently, the choices for this sample were for the Be doping to be the minimum we could MBE dope and for the *n*-type layer to be unintentionally doped.

The surface morphology was exceptionally good with minimum visible surface defects. Figure 33 shows a Nomarski optical microscope image of the surface morphology. The debris shown in the center was used for focusing and it was very hard to find defects of any kind. The first processing step was the deposition of a top ohmic Ti/Pt/Au metalization using a lift-off photolithography process. The mesa etch down to 6400 Å from the top layer was performed using the metal as an etch mask. The bottom Ti/Pt/Au metalization was deposited for conducting the InAs:NID layer. The devices were tested with the metalizations as deposited, i.e., there was no sintering of the ohmics or any thermal treatment. The I-V characteristics indicated high leakage currents extremely weak rectification and basically a resistor-like behavior. Figures 34 and 35 show some examples.

Sample R000823N was one of the last samples grown before the MBE system was down for repairs, partially to replenish the Ga source and to repair the shutter. The Ga source partial depletion resulted in unstable Ga fluxes. There was a lingering uncertainty if the Ga problem affected this sample. Further etching down to the InAs-n substrate was done, for a total depth of 1.3 μm; testing indicated no diode characteristics. Etching back to the substrate was performed to determine if the MBE-grown layers were all accidentally *p*-type, in which case a diode would form between the MBE-grown layers and the *n*-type substrate. This apparently is not the case. Some of the observed I-Vs are shown in Figs. 35 and 36. The measured current for the processed devices does not scale with area but rather shows a strong dependence

on the distance between the contacts (Figs. 37 to 42). Typing of the substrate suggests *n*-type material, i.e., no *p*-type rectification was observed (Fig. 43).

In the absence of any additional analytical work on sample R000823N, the conclusion from the work on this sample is that the intended lightly doped Be layer is not electrically active. This might be as a result of insufficient compensation of the background *n*-type doping in InAs. On a happier note, unlike other InAs samples, the crystalline quality and surface morphology is exceptionally good for the NRL MBE samples.

Samples examined later, however, showed that SIMS background doping investigation on the NRL MBE system indicated severe Fe contamination at the time the InAs structures for this study were grown. Consequently, the doping for the samples examined in this study were strongly compensated, as the electrical characteristics suggest.

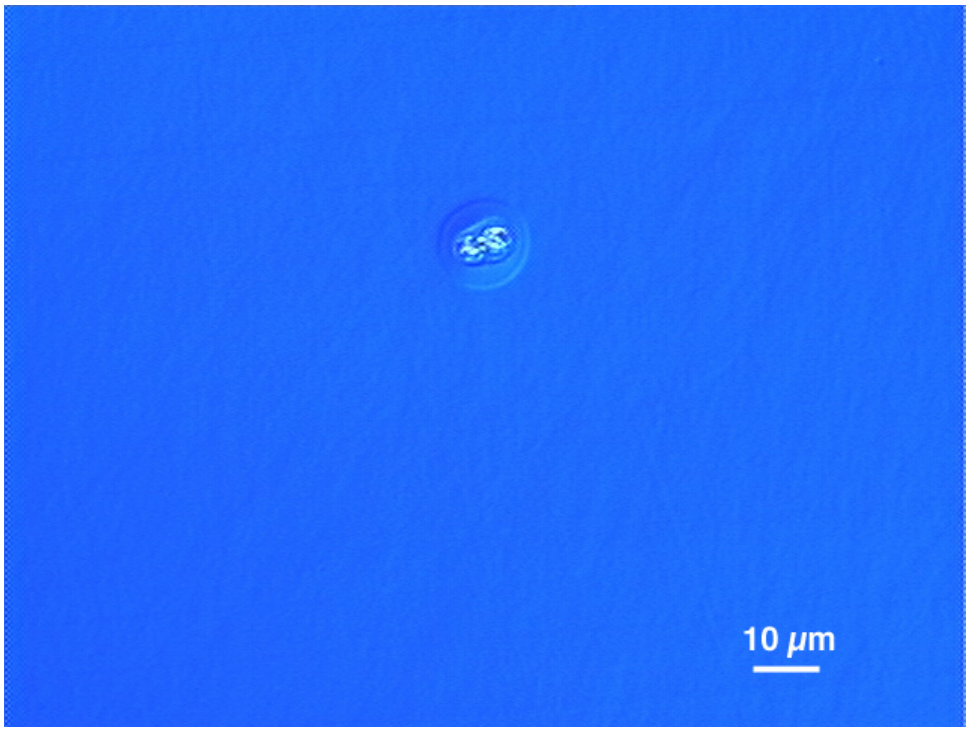

Fig. 33 — Nomarski optical microscope image of the surface morphology of sample R000823N. The surface morphology was exceptionally good with minimal visible surface defects. The debris shown in the center was used for focusing. The rings around this defect suggest that the debris was on the surface during the growth. Nevertheless, it was very hard to find defects of this or any other kind.

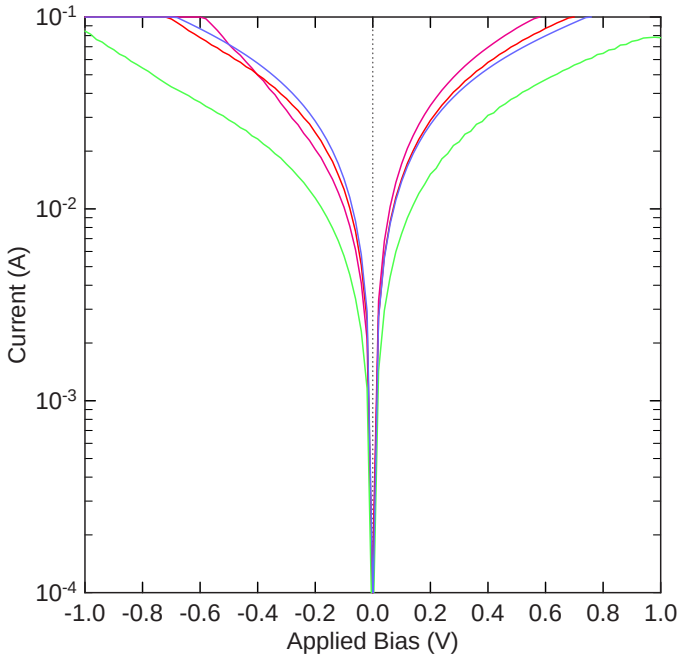

Fig. 34 — I-V characteristics from "diodes" of different sizes on sample R000823N. Ohmic-like behavior was exhibited.

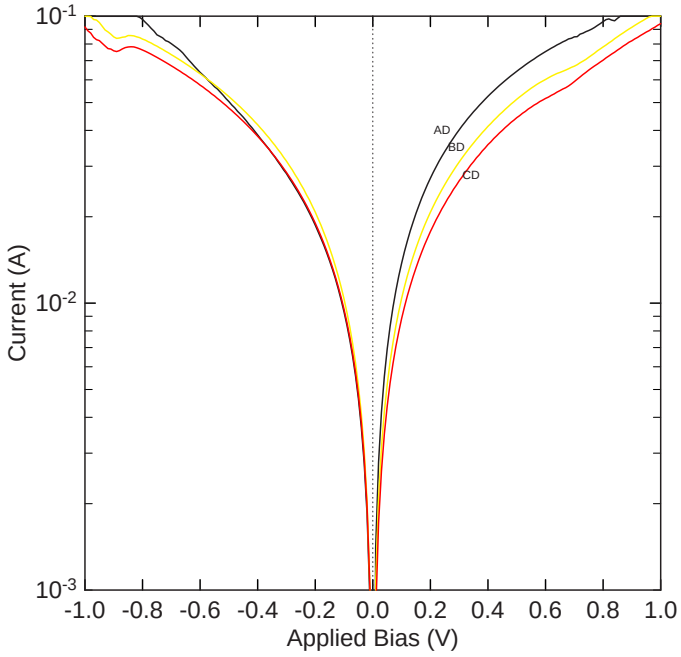

Fig. 35 — I-V characteristics of back-to-back "diodes" between diodes A, B, C, and D. Diode D is on ground potential. Dimensions for the diodes are A: 315 μm × 315 μm; B: 155 μm × 155 μm; C: 79 μm × 79 μm; and D: 40 μm × 40 μm.

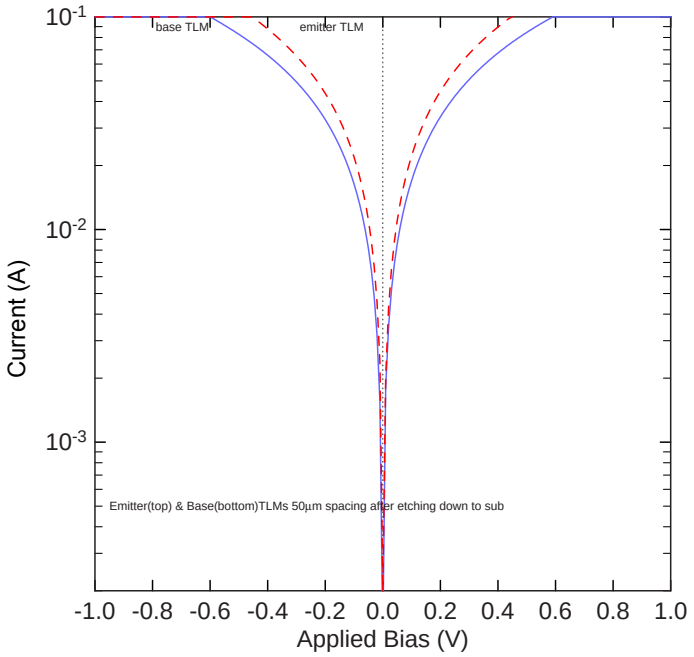

Fig. 36 — Current voltage characteristics for sample R000823N of top-contact TLMs with the nominally *p*-type material between the metal contacts removed down to the *n*-type substrate, resulting in two back-to-back diodes connected by the substrate. The bottom-contact TLM is ohmic on the base layer. Notice that both contacts behave similarly ohmic without any back-to-back diode behavior from either contact.

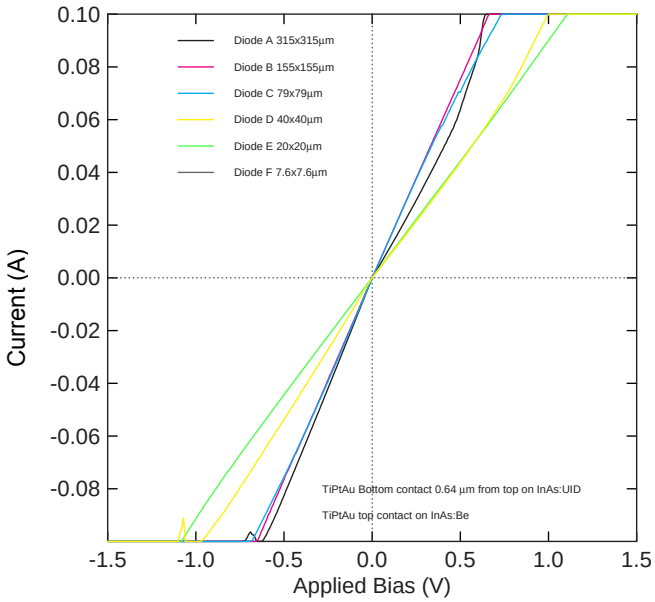

Fig. 37 — Current voltage characteristics after etching the material between the contacts down to the substrate layer. If a *p/n* junction was involved between the epi-layer and substrate, the I-V characteristics would have been similar to two back-to-back diodes.

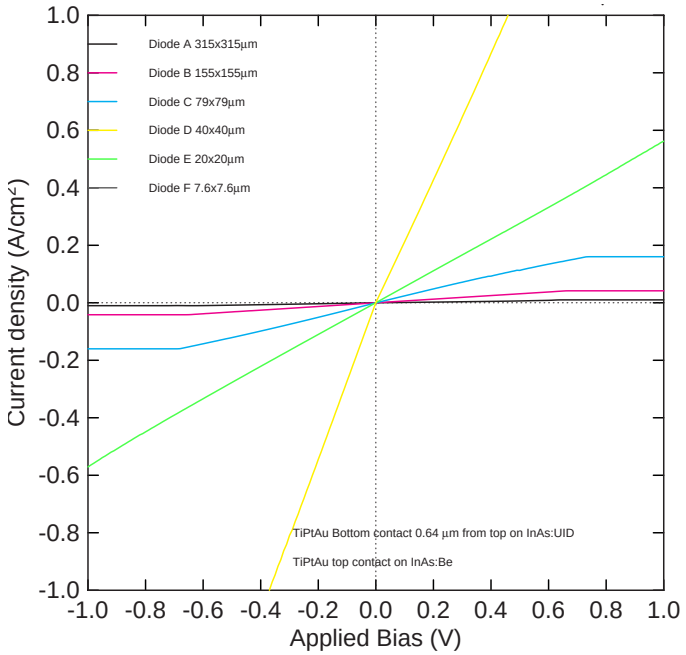

Fig. 38 — R00823N devices A through C after etching the material between the top and bottom contact down to the substrate (1.3 µm). The Y scale is normalized to the individual device area. The measured current has no area dependence.

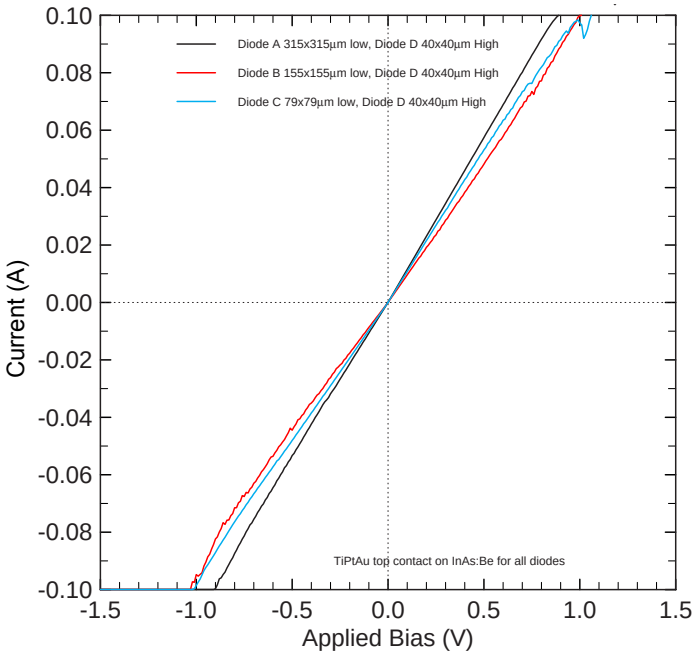

Fig. 39 — R00823N current voltage characteristics between devices A through C and device D after etching the material between the top and bottom contacts down to the substrate (1.3 µm).

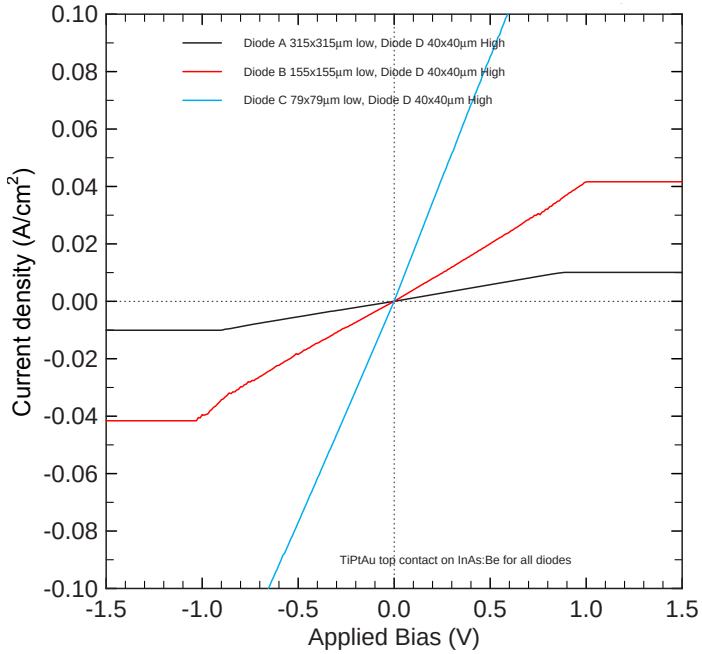

Fig. 40 — R00823N current voltage characteristics between devices A through C and device D (small area) after etching the material between the top and bottom contact down to the substrate (1.3 µm). The Y scale is normalized to the area of each device. There is obviously no area dependence on the current observed.

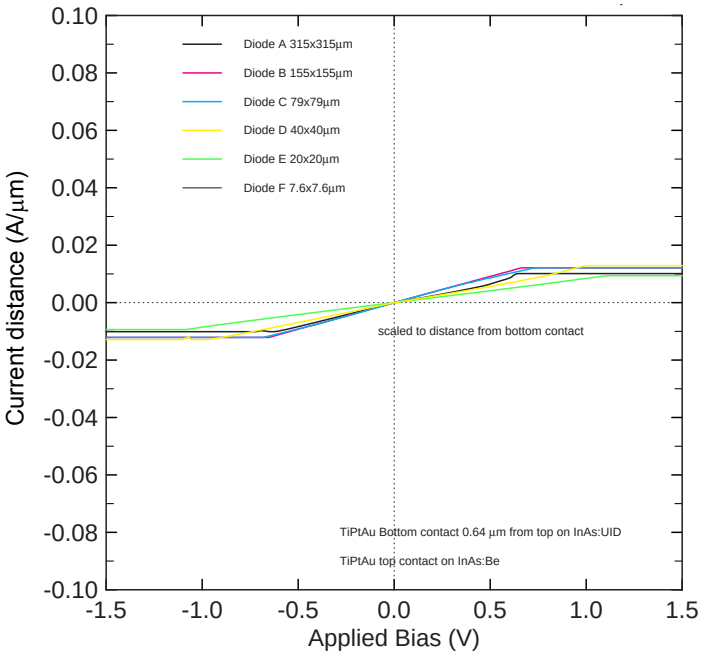

Fig. 41— R000823N devices after etching down to the substrate (1.3 µm). The Y axis shows the current scaled to the distance between the top and bottom contact spacing.

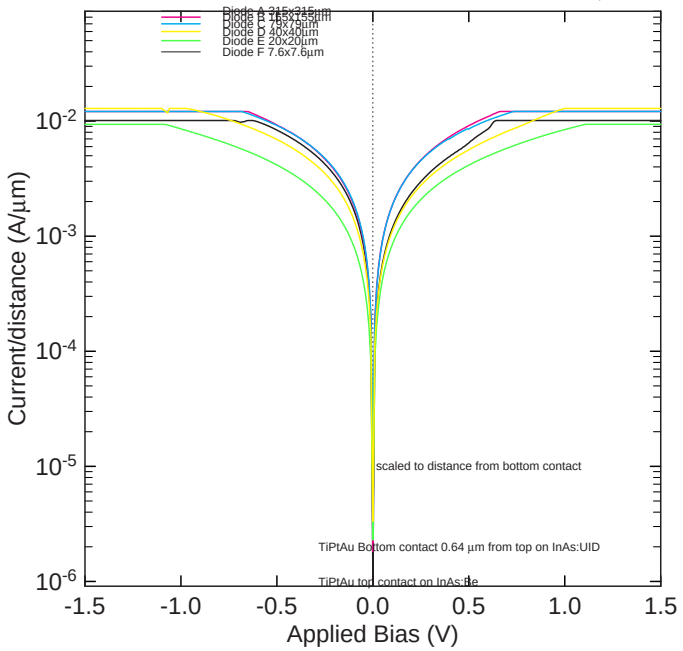

Fig. 42 — More detail of the plot of Fig. 41 for R000823N devices after etching down to the substrate (1.3 µm). The Y axis shows the current scaled to the distance between the top and bottom contact spacing.

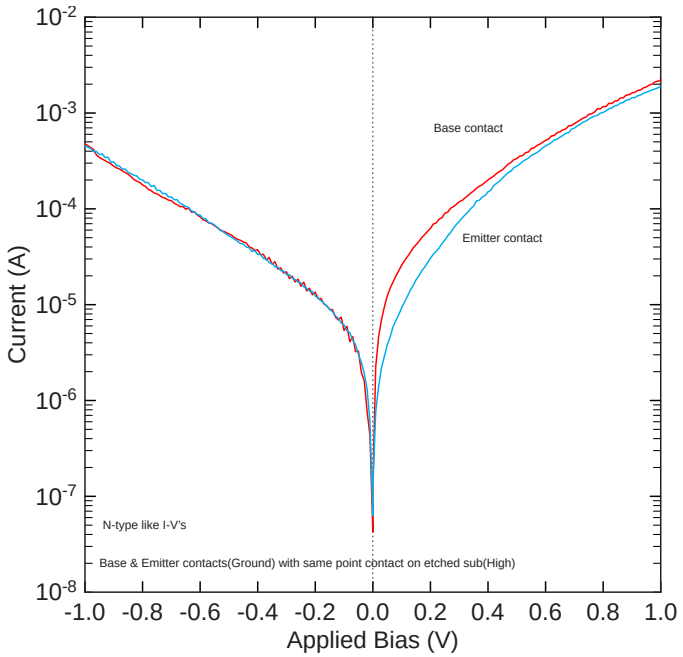

Fig. 43 — Point probe contact on etched substrate of R000823N with smaller area and other contact on ohmic metal of emitter (blue line) or base (red line) result in higher current in forward bias (*n*-type-like) characteristics, confirming an *n*-type substrate

5.5 The Final InAs *p/n* Junctions

The cumulative knowledge of the previous InAs structures leads to one of the most interesting and desired results from the final sample UR 2820 grown at the University of Rochester used in this work. The nominal structure layer is shown in Table 1. Notice that the collector buffer for this sample is considerably thicker, (1.5 μm) and not intentionally doped. The I-V characteristics of this sample are shown in Fig. 44. For processing, Ti/Pt/Au universal ohmics for both the top *p* and bottom *n* contacts was used. The mesa was etched with the emitter metalization as a mask down to 4,400 Å. To account for the possibility of dopant distribution during the growth (based on the earlier SIMS analysis) and to ensure bottom layer contact, the mesa was etched beyond the nominal *p*+/*p* layer thickness (1000 Å/2000 Å).

The diode ideality factors range from 1 to 1.8 along the 0 to 1 V forward bias, as can be seen in Fig. 45, suggesting a combination of mainly drift/diffusion with some recombination/generation current transport mechanism. The reverse leakage current is the best we have seen so far with the best device having as low as 13 μA at –1 V (Fig. 46). When the diode area is accounted for in the current density, the forward bias characteristics do not have any significant size dependence for low biases, as shown in Fig. 47. The reverse bias leakage current appears to be largely dependent on edge effects and structural defects within the area that act as strong generation/recombination centers.

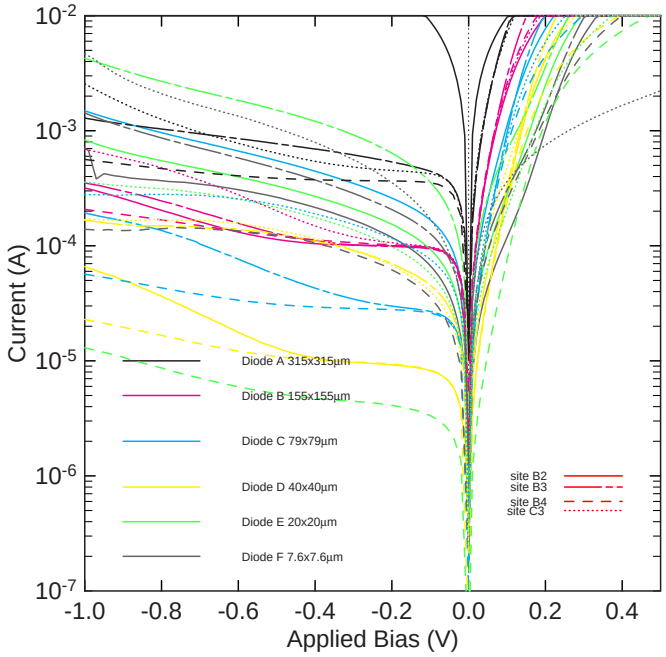

Fig. 44 — I-V characteristics from devices tested on sample UR2820. Shown are sites B2, B3, B4, and C3, with six different junction areas.

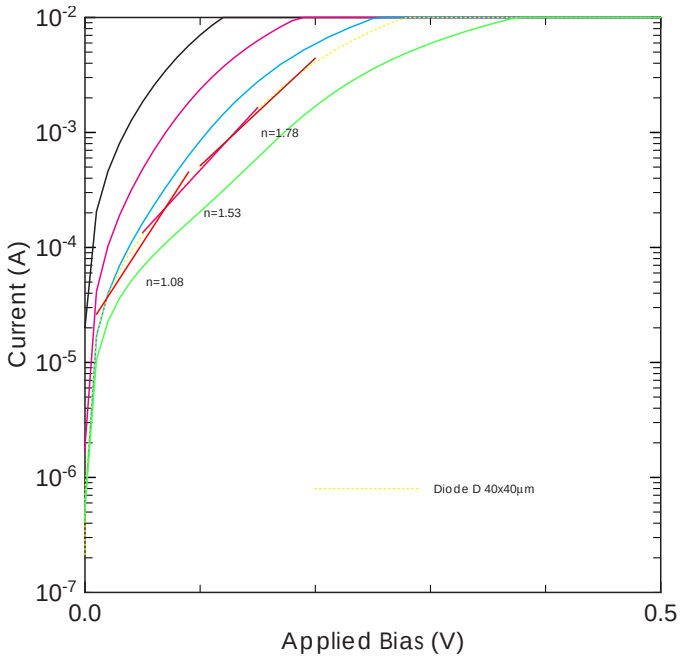

Fig. 45 — Forward-bias ideality factors for site C3 device D. Devices A through E forward characteristics show similar ideality factors.

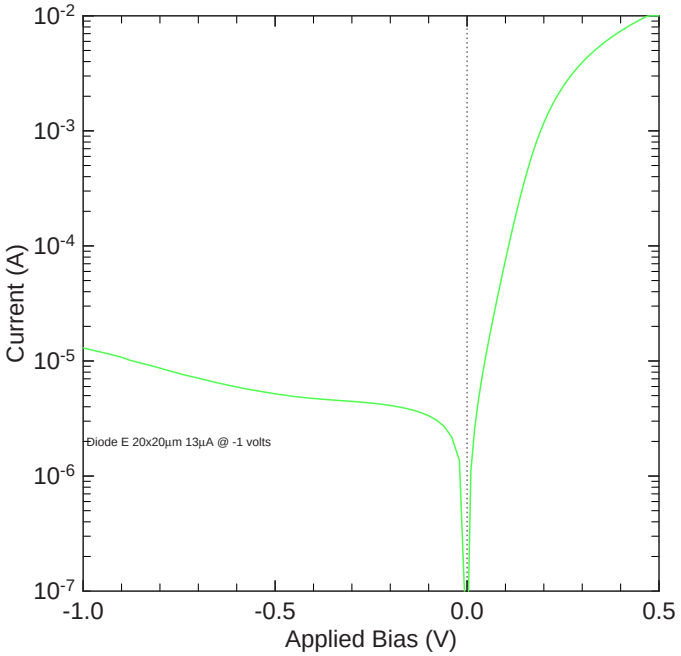

Fig. 46 — Device with low reverse bias leakage current for sample UR2820. Shown is site B4, device E.

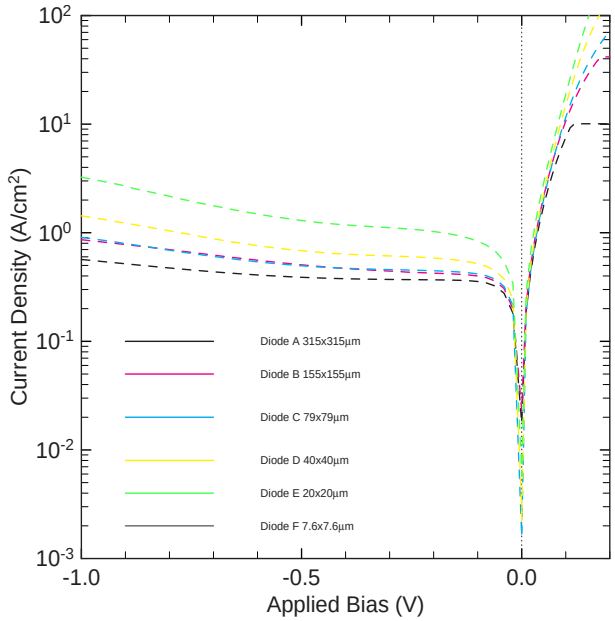

Fig. 47 — Area-normalized I-V characteristics of sample UR2820. Note the very high current density achieved with the InAs devices. The forward bias current scales with area for low bias levels. At higher forward bias levels, series resistance and self-heating effects dominate. The current compliance for the HP system employed for these measurements limits the testing of these devices at higher current levels. The reverse bias leakage current is mostly recombination center (defect) related.

The reverse breakdown voltage is also impressive for InAs. In some devices we were able to get it up to -6.5 V, as can be seen in Fig. 48. We have noticed that for the best reverse breakdown devices, a semicatastrophic breakdown occurs at higher biases. When this happens, the device still rectifies but with a higher leakage current and a reproducible breakdown voltage near -1 to -1.5 V (Figs. 49 and 50). We were able to correlate the lower leakage currents to devices with significantly small numbers of large defects as observed by optical microscope (Fig. 51). The devices that originally (first I-V trace) exhibited high leakage currents and low reverse breakdown voltages usually exhibited large structural defects (Figs. 52 and 53).

Conventional belief would suggest that the InAs material can withstand the large reverse bias and that the current conduction mechanism along the structural defects is responsible for the premature breakdown and increased leakage current. The fact, however, that the semicatastrophic breakdown occurred at higher biases and then the device became leaky with a reversible breakdown around 1 to 1.5 V is suspicious. Defects are known to behave in very unpredictable ways and it is conceivable that some may act as recombination (current sinks), resulting in the observed low leakage current. Under this hypothesis, when the conduction along the defect is established, the semicatastrophic voltage breakdown is observed and the material reverts to its original low-Vbd tunneling mechanism. Alternatively, in the conservative approach, the largely defect-free material can withstand the observed high reverse breakdown. When the avalanche multiplication takes place, conduction along the defect is permanently altered, resulting in a premature tunneling-defect-related breakdown with a 1 to 1.5 Vbd.

Considering the small energy bandgap of InAs as analogous to what is known for other small bandgap semiconductors (like Ge), a breakdown voltage below 4 Eg = 1.448 V would be due to a band-to-band tunneling in junctions with high doping concentrations, while a breakdown voltage over 6 Eg = 2.172V is due to impact ionization. In the impact ionization regime, assuming a maximum critical electric field of 9×10^4 V/cm [7], with an intrinsic carrier concentration for InAs of 9.2e-14, the highest breakdown voltage we can expect is 35.5 V. For an electron residual background concentration of 1e16, the breakdown can be between 3.27 V and 32.7 V for 1e15 background doping. So it is possible that low enough background doping in the NID InAs layer can sustain the observed high breakdown voltages. It will be very useful to have some SIMS analysis performed on the current samples to establish the background concentration achieved since earlier SIMS results suggested a rather high 1e17 NID doped concentration.

In fact, an unusual defect-related behavior warrants further investigation. Figure 54 shows the I-V characteristics of two adjacent ohmic contacts on the top surface separated by a 50-μm gap, just before the mesa etching. The I-V in this case is expected to be simple, linear, and resistor like. Nevertheless, one of the contacts had a visible defect, resulting in the abnormally sharp current increase at about 1 V. The polarity of the sharp current increase depends on the polarity on the contact with the visible defect and the defect conduction appears to be unidirectional. Figure 55 shows the I-V for the same 50-μm-spaced contacts after etching about 1600 Å. The I-Vs were expected to be linear until we etch down to the *p/n* junction interface when it will turn to a symmetric back-to-back diode. At 1600 Å, according to the layer specifications, we should be in the *p*-layer. The depletion region of a *p*-/low-*n* layer would mainly extend along the lower doped *n*-layer. Nevertheless, the I-V appears diode-like and the sharp current increase occurs again at about 1.2 V. The asymmetry of the I-V can be explained by the defects causing a different current path for one of the contacts. The higher resistance on the defect side can be either due to increased recombination along the defect or to a localized depletion region around the defect. Etching down to 4400 Å, i.e., ensuring that we are forcing the current through the *p/n* junction interface through the NID layer, the contact-to-contact I-V still appears as a rectifying contact with the sharp current increase happening again around 1.2 V, as shown in Fig. 56. Checking the I-Vs between the contact with the

visible defect and a similar contact 30 μm away, the sharp current increase polarity inverts (now the high bias is on the contact with the defect), but the other side (the new contact) does not exhibit a reverse breakdown up to the 2 V tested (Fig. 57).

The sharp breakdown not being affected by the etching depth suggests that the junction is not involved in the breakdown mechanism, i.e., defect causing the 1.2 V breakdown runs from the surface through the junction. Defect conduction works in strange ways and additional work is needed in order to understand it. Nevertheless, the UR2820 *p/n* junction characteristics are what we would like to see in the base collector junction for an InAs bipolar transistor. Further tests include *n*-type InAs and InAlAs on *p*-type structures to ensure that the bottom *p* on *n* does not deteriorate during the growth of the top emitter. Subsequent testing will incorporate these layers in HBT and P-BJT transistor structures. A goal of future improvement is the reduction of defects.

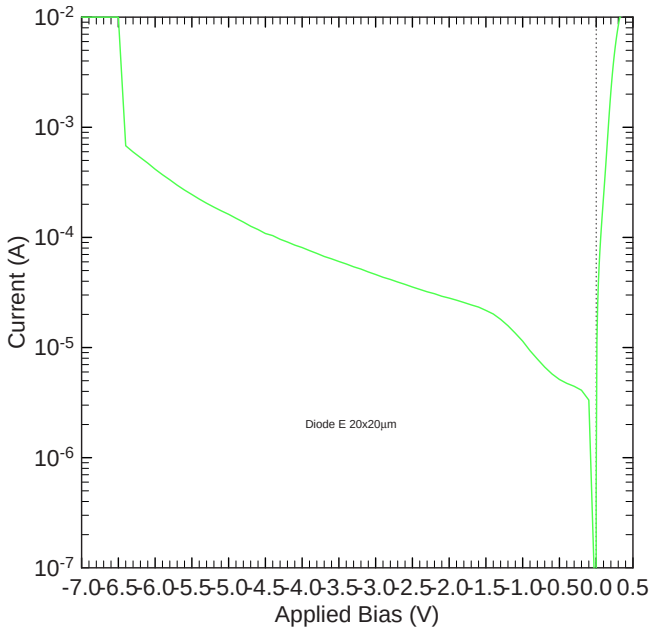

Fig. 48 — Sample UR2820 device site B4 device E at high reverse bias levels

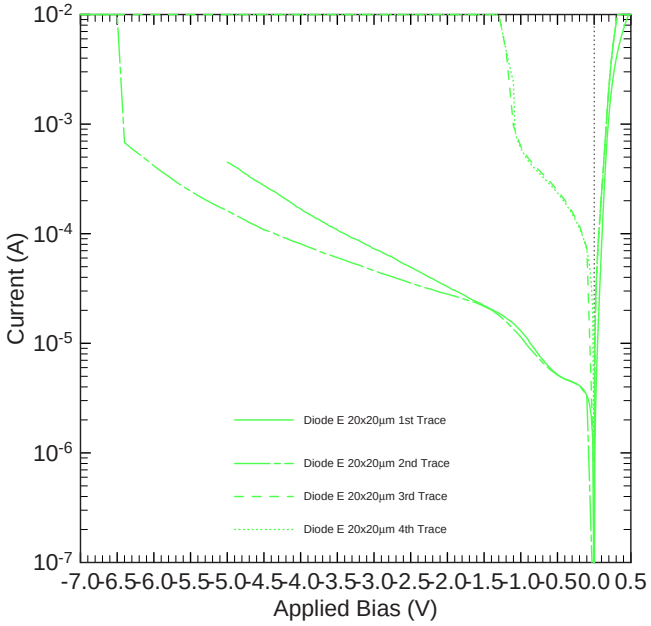

Fig. 49 — Reverse breakdown characteristics of diode B4-E from sample UR2820. Note that reverse bias is repeatable until a semicatastrophic breakdown occurs at high voltage levels, after which the diode has a higher leakage current with a repeatable breakdown of around 1 V.

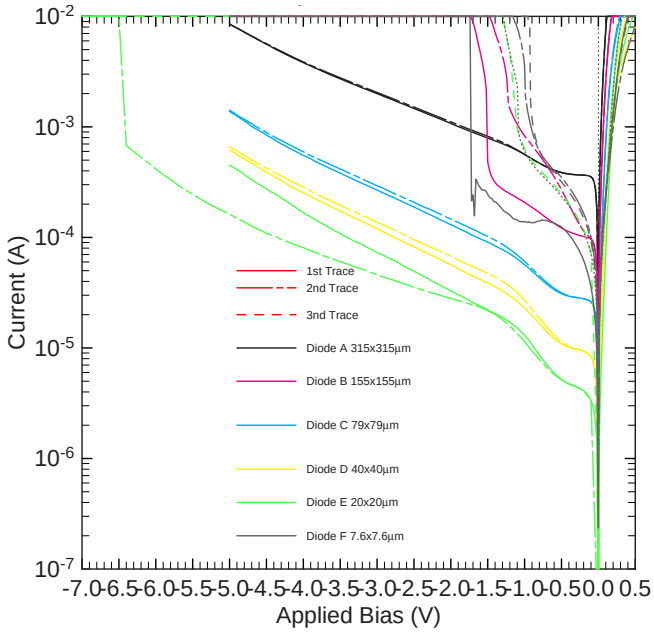

Fig. 50 — Sample UR2820 reverse breakdown characteristics are stable before and after the semicatastrophic breakdown. The reverse leakage current is less before the semicatastrophic breakdown, which ranges from 1.5 to 6.5 V and appears to be defect related.

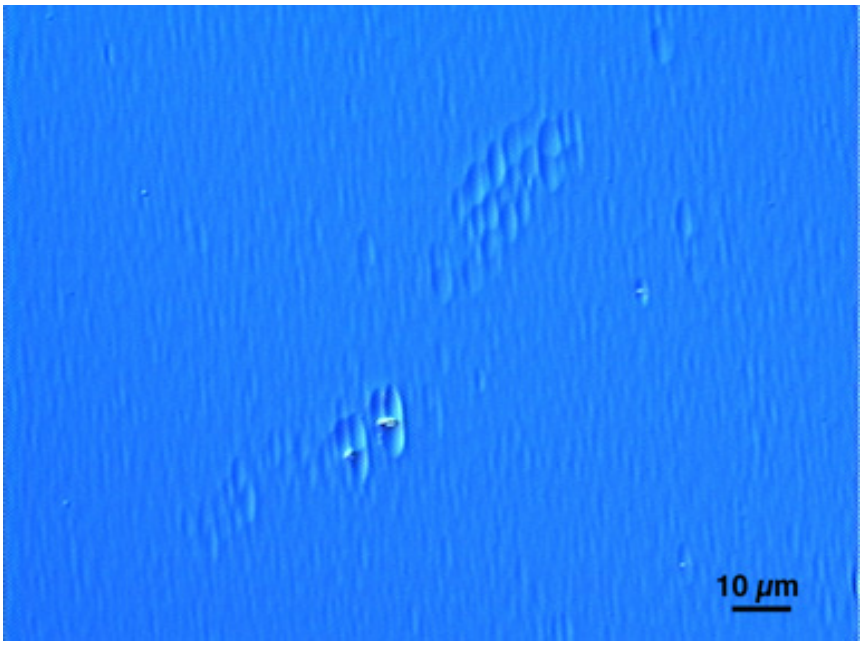

Fig. 51 — Nomarski optical microscope image of sample UR2820 before processing. The surface has a visible texture, reminiscent of the InP "rice" surface texture encountered in that material's early developmental stages. There are a number of large structural defects that appear to originate on point defects.

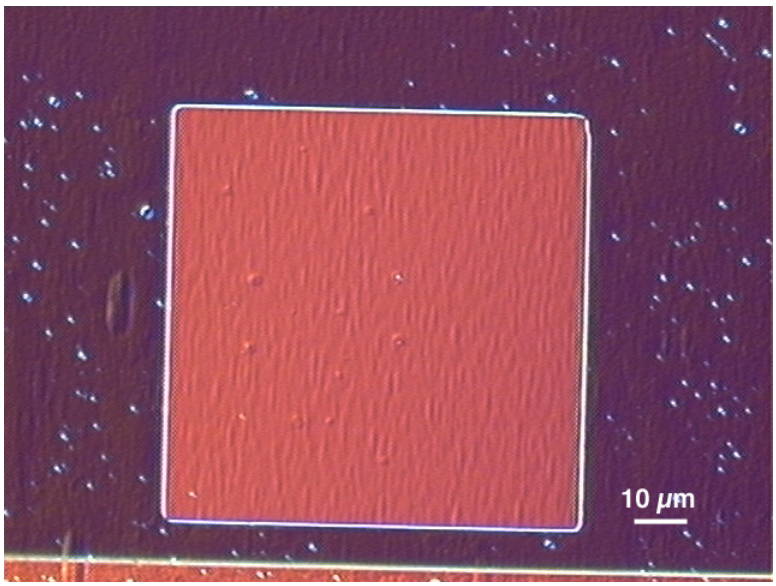

Fig. 52 — Nomarski optical microscope image of a processed *p/n* junction showing the top metal contact. Although there are some structural variations on the surface of this device, no large surface defects are visible. Shown is site B1, device C.

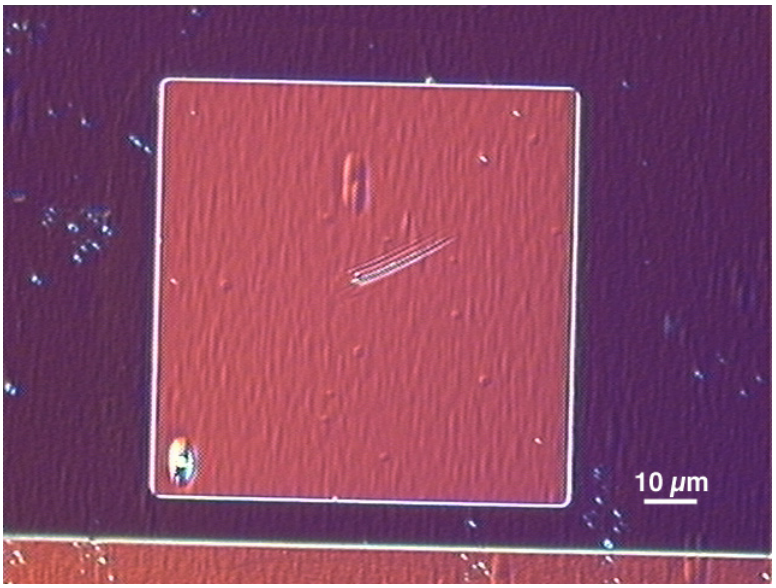

Fig. 53 — Nomarski optical microscope image of a processed *p/n* junction showing the top metal contact with visible large structural defects that are believed to be responsible for the reverse bias behavior. Shown is site B2, device C.

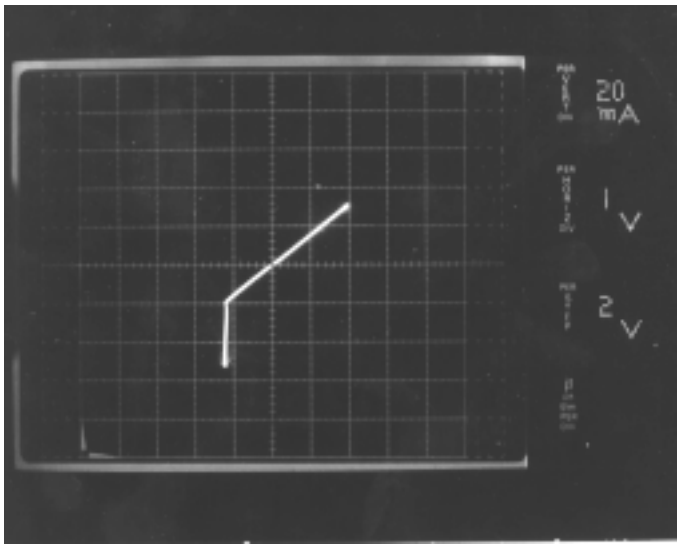

Fig. 54 — I-V characteristics of two adjacent ohmic contacts on the top surface separated by a 50-μm gap, just before the mesa etching. The I-V in this case is expected to be simple, linear, and resistor-like. One of the contacts had a visible defect that might be responsible for the abnormally sharp current increase at about 1.2 V.

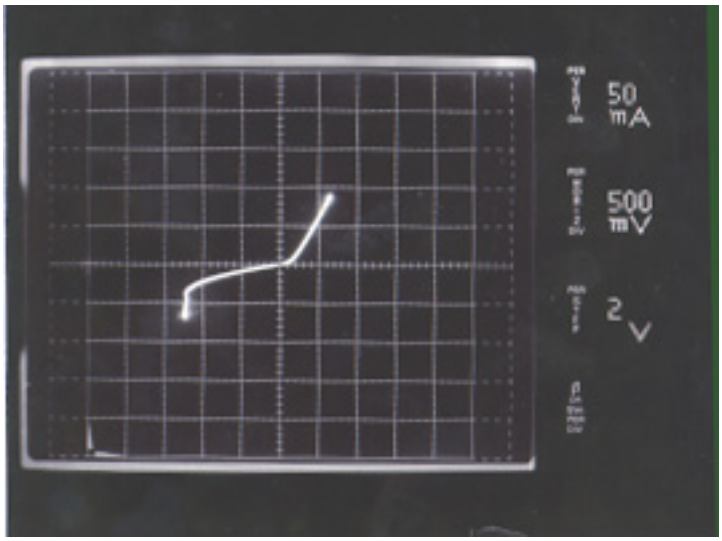

Fig. 55 — I-V characteristics for the same 50-μm spaced contacts of Fig. 54 after etching about 1600 Å down. The sharp current increase now happens at about 1.3 V.

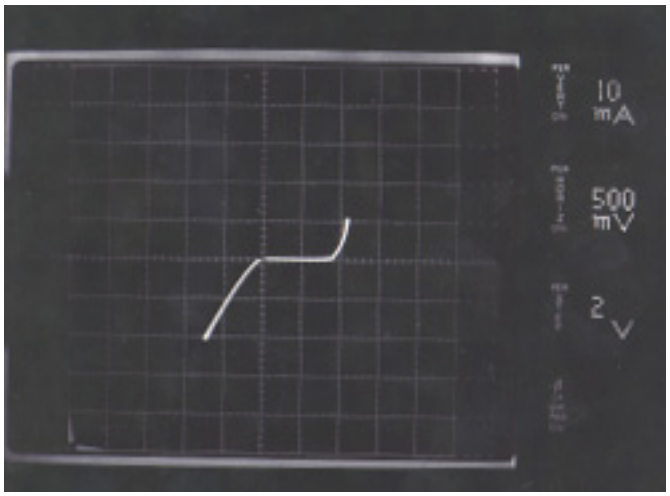

Fig. 56 — I-V for the same 50-μm spaced contacts of Fig. 54 after etching about 4400 Å down to the NID layer. The sharp current increase happens at about 1.2 V.

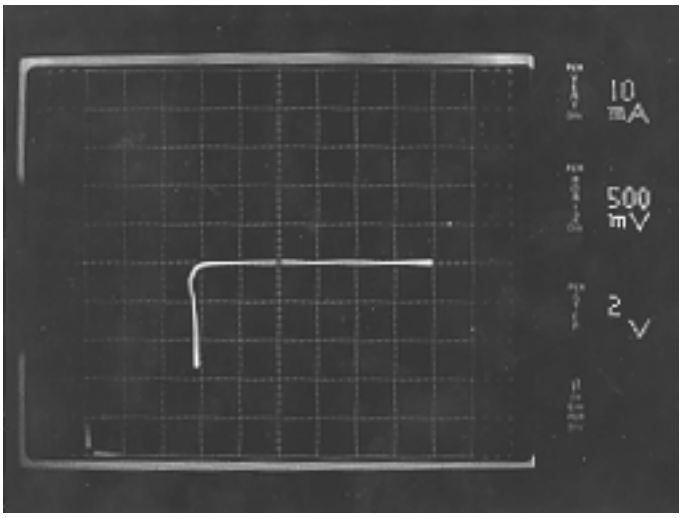

Fig. 57 — I-V characteristics between the defect-containing contact and a new third contact spaced 30 μm away. The new contact does not appear to break down up to the tested 2-V bias.

6. FUTURE DIRECTIONS

The work performed here is the prelude of a continuing effort in developing advanced devices in exploratory materials. InAs along with the Sb-containing alloys have extremely promising properties for advancing the performance of high-speed, low-power dissipation devices and fulfilling the expectations of the next generation of the Navy's and the Nation's communication needs. The knowledge in device processing and material growth accumulated from this work will be directly applied to the development of bipolar transistors suitable for high-density integrated circuits.

7. ACKNOWLEDGMENTS

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